

Compal Confidential

Lotus AMD M/B LA8731P Schematics Document

AMD Trinity APU / Hudson FCH M3



Date : 2011-12-27

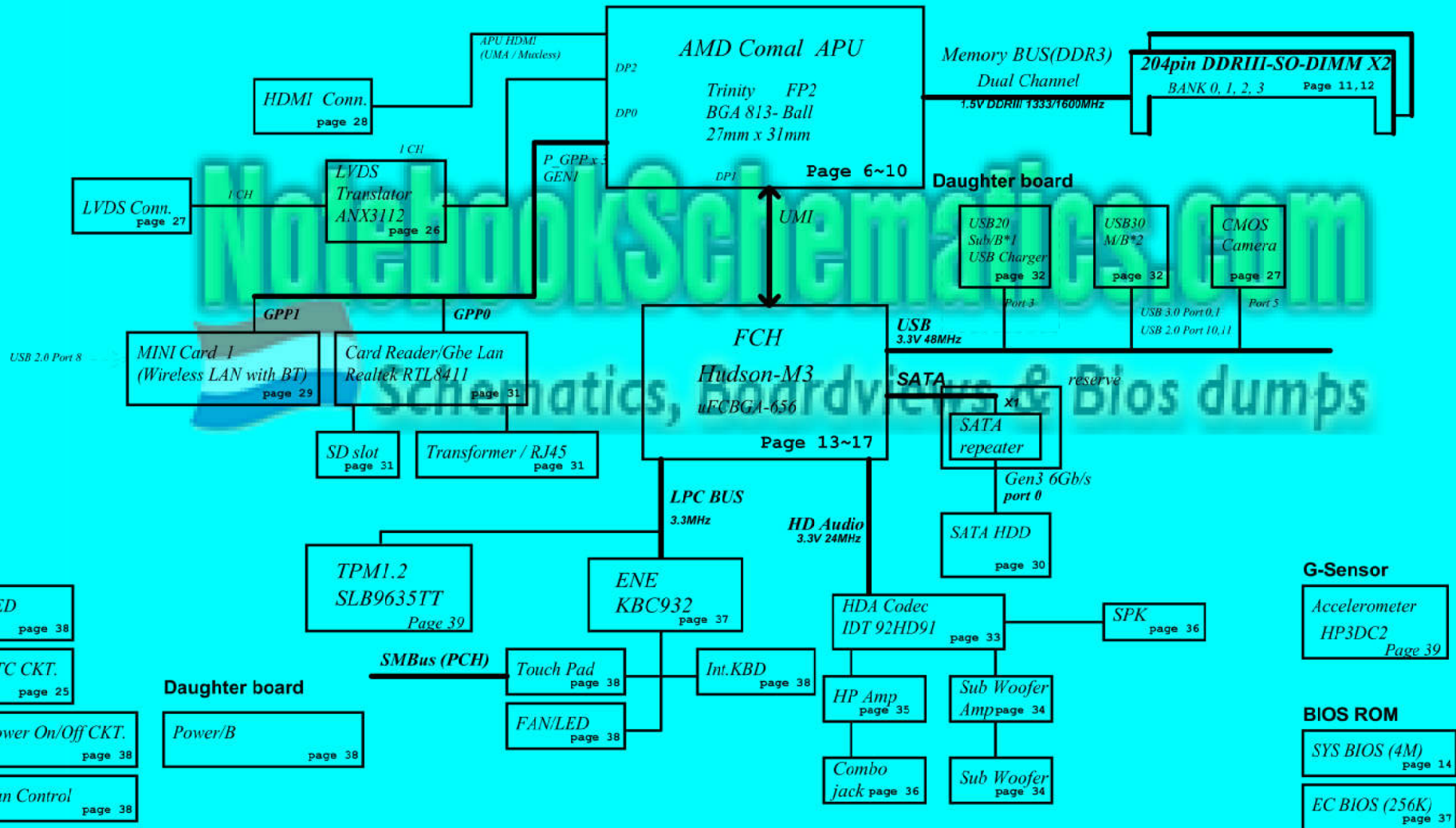
Version 0.1

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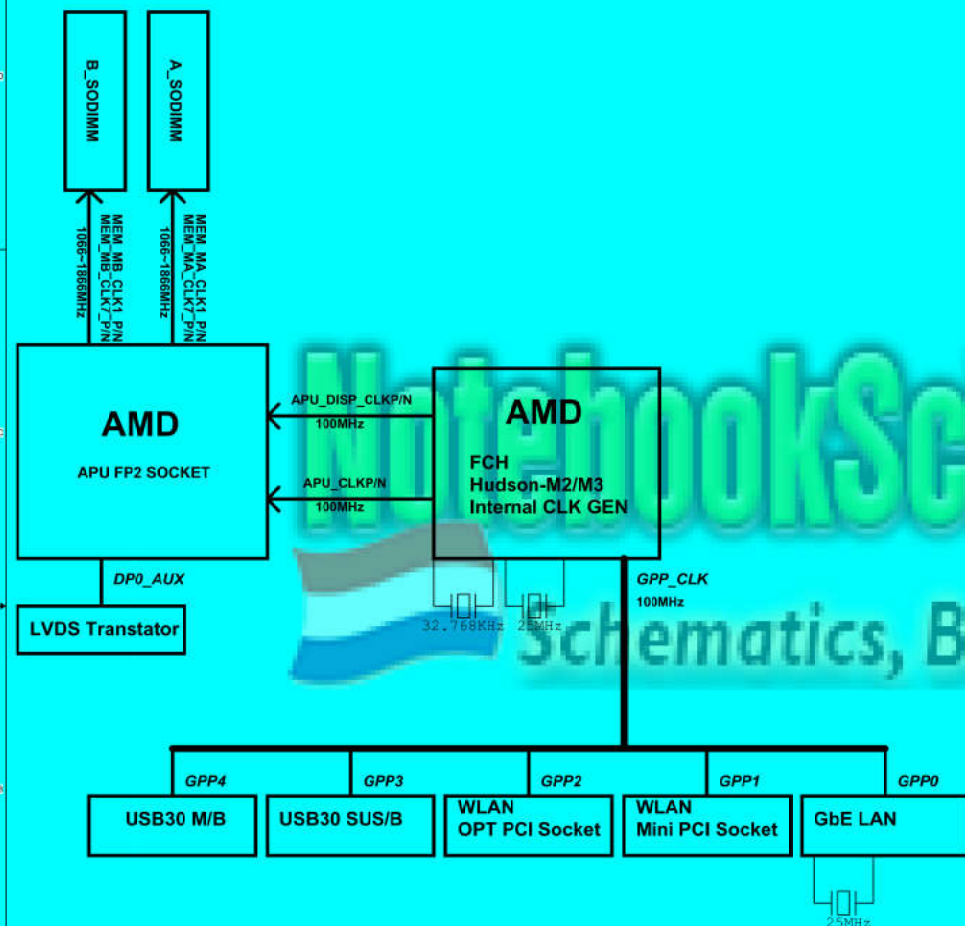
Model Name : QAU51 AMD

AMD Comal

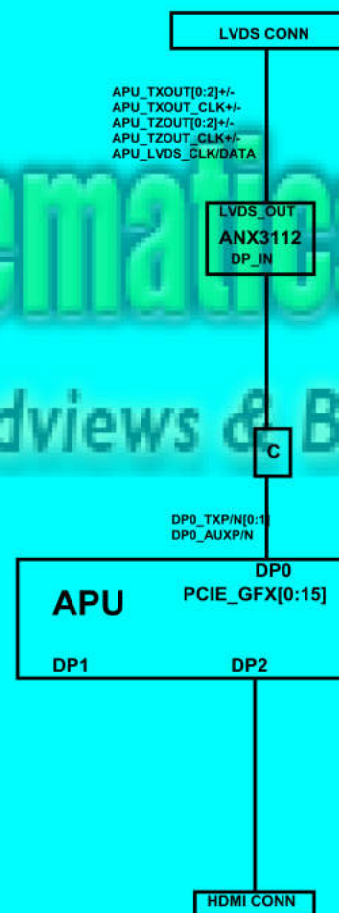


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CLOCK DISTRIBUTION



DISPLAY OUTPUT



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Audio Codec SSID

Platform	Platform ID
Evora 1.0 UMA	0x18DE

x = 1 is read cmd, x = 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR(RTD-2132S)	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	90			
DDR DIMM2	1101 001X b	94			

FCH SM Bus 1 address

Device	Address	HEX	Device	Address	HEX

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board id	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Option Table

BOM Structure	Description
---------------	-------------

BOM Config

UMA
V

USB Port Table

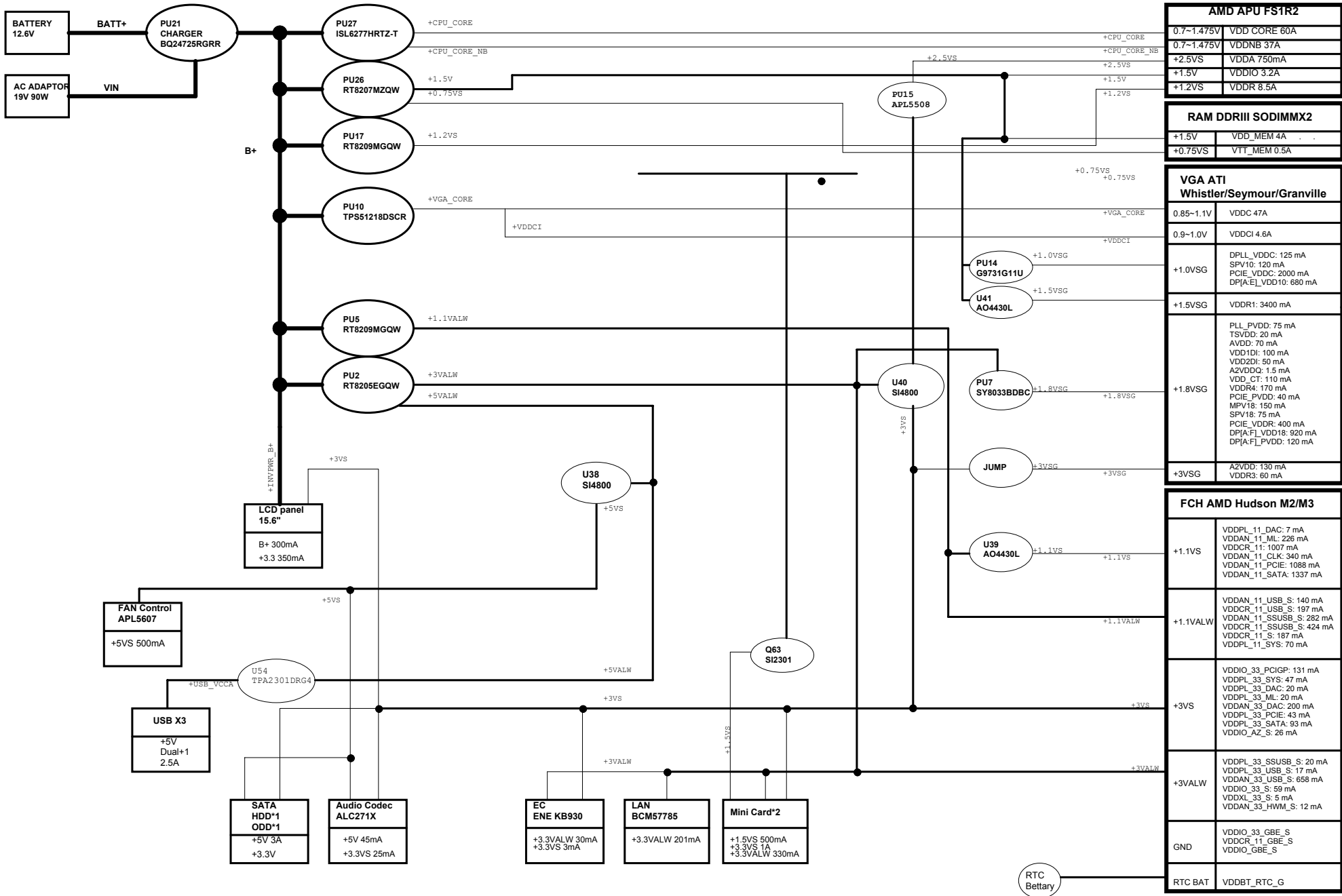
USB 2.0	USB 1.1	Port	1 External USB Port
	UHCI0	0	USB2.0 (left side)
		1	
EHCI1	UHCI1	2	
		3	
	UHCI2	4	
		5	Camera
		6	
	UHCI3	7	
		8	BT
		9	
EHCI2	UHCI5	10	USB2.0 (Right side)
		11	USB2.0 (Right side)
		12	
	UHCI6	13	

USB 3.0	Port	1 External USB Port
	0	USB3.0 (Right side)
	1	USB3.0 (Right side)
	2	
	3	

SMBUS Control Table

	SOURCE	BATT	Charger	HP Amp	MINI3	SODIMM	EC_SMB_CK2 EC_SMB_DA2	EC_SMB_CK1 EC_SMB_DA1	G-Sensor	TP
EC_SMB_CK1 EC_SMB_DA1	KB932	V	V						V	
EC_SMB_CK2 EC_SMB_DA2	KB932			V						
FCH_SCLK0 FCH_SDATA0	FCH					V				
FCH_SCLK1 FCH_SDATA1	FCH									V

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AMD APU FS1R2	
0.7~1.475V	VDD CORE 60A
0.7~1.475V	VDDNB 37A
+2.5VS	VDDA 760mA
+1.5V	VDDIO 3.2A
+1.2VS	VDDR 8.5A

RAM DDRIII SODIMMX2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCIE_VDDC: 2000 mA DP[A:E]_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1DI: 100 mA VDD2DI: 50 mA A2VDDQ: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCIE_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCIE_VDDR: 400 mA DP[A:F]_VDD18: 920 mA DP[A:F]_PVDD: 120 mA
+3VSG	A2VDD: 130 mA VDDR3: 60 mA

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIEP: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

VRAM 512/1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

UCPU1A

GPU

Delete GPU
1202 CalvinGLAN/Card reader
WLAN

UMI

AP1	P_GFX_RXP[0]	P_GFX_TXP[0]	AN1
AP2	P_GFX_RXN[0]	P_GFX_TXN[0]	AN2
AM1	P_GFX_RXP[1]	P_GFX_TXP[1]	AM4
AM2	P_GFX_RXN[1]	P_GFX_TXN[1]	AM3
AK3	P_GFX_RXP[2]	P_GFX_TXP[2]	AK2
AK4	P_GFX_RXN[2]	P_GFX_TXN[2]	AK1
AI1	P_GFX_RXP[3]	P_GFX_TXP[3]	AH1
AJ2	P_GFX_RXN[3]	P_GFX_TXN[3]	AH2
AH4	P_GFX_RXP[4]	P_GFX_TXP[4]	AE3
AI3	P_GFX_RXN[4]	P_GFX_TXN[4]	AE4
AE2	P_GFX_RXP[5]	P_GFX_TXP[5]	AE1
AF1	P_GFX_RXN[5]	P_GFX_TXN[5]	AE2
AD1	P_GFX_RXP[6]	P_GFX_TXP[6]	AD4
AD2	P_GFX_RXN[6]	P_GFX_TXN[6]	AD3
AB3	P_GFX_RXP[7]	P_GFX_TXP[7]	AB2
AB4	P_GFX_RXN[7]	P_GFX_TXN[7]	AB1
AA1	P_GFX_RXP[8]	P_GFX_TXP[8]	Y1
Y4	P_GFX_RXN[8]	P_GFX_TXN[8]	V3
Y3	P_GFX_RXP[9]	P_GFX_TXP[9]	V4
V2	P_GFX_RXN[9]	P_GFX_TXN[9]	V2
V1	P_GFX_RXP[10]	P_GFX_TXP[10]	V1
T1	P_GFX_RXN[10]	P_GFX_TXN[10]	T4
T2	P_GFX_RXP[11]	P_GFX_TXP[11]	T3
P3	P_GFX_RXN[11]	P_GFX_TXN[11]	P2
P4	P_GFX_RXP[12]	P_GFX_TXP[12]	P1
N1	P_GFX_RXN[12]	P_GFX_TXN[12]	M1
N2	P_GFX_RXP[13]	P_GFX_TXP[13]	M2
M4	P_GFX_RXN[13]	P_GFX_TXN[13]	K3
M3	P_GFX_RXP[14]	P_GFX_TXP[14]	K4
K2	P_GFX_RXN[14]	P_GFX_TXN[14]	J1
K1	P_GFX_RXP[15]	P_GFX_TXP[15]	J2
	P_GFX_RXN[15]	P_GFX_TXN[15]	

GRAPHICS

GPU

UMI

Delete GPU
1202 Calvin

GPU

GLAN/Card reader
WLAN

UMI

AG7	PCIE_FTX_DRX_P0	CC33	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_P0	23
AG8	PCIE_FTX_DRX_N0	CC34	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_N0	23
AE7	PCIE_FTX_DRX_P1	CC35	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_P1	21
AE8	PCIE_FTX_DRX_N1	CC36	1	2	.1U 0402 16V7K	PCIE_FTX_C_DRX_N1	21

AN6	UMI_FTX_MRX_P0	CC37	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P0	13
AM6	UMI_FTX_MRX_N0	CC38	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N0	13
AP6	UMI_FTX_MRX_P1	CC39	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P1	13
AB6	UMI_FTX_MRX_N1	CC40	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N1	13
AP4	UMI_FTX_MRX_P2	CC41	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P2	13
AR4	UMI_FTX_MRX_N2	CC42	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N2	13
AP3	UMI_FTX_MRX_P3	CC43	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_P3	13
AR3	UMI_FTX_MRX_N3	CC44	1	2	.1U 0402 16V7K	UMI_FTX_C_MRX_N3	13

+1.2VS O
RC1 196_0402_1% P_ZVDDP

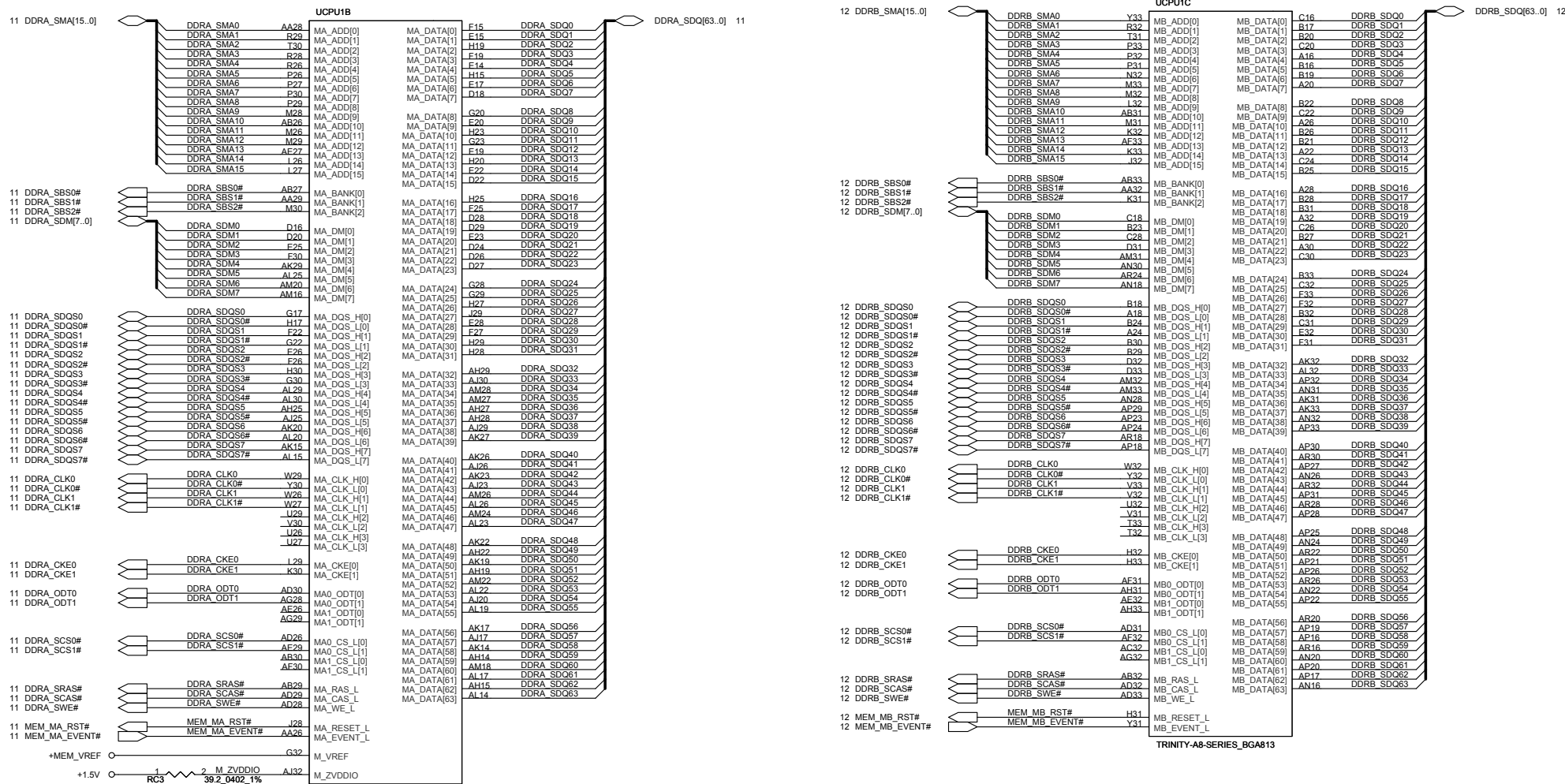
P_ZVDDP W/S=8/12 mil, <3000mil

TRINITY-A8-SERIES_BGA813

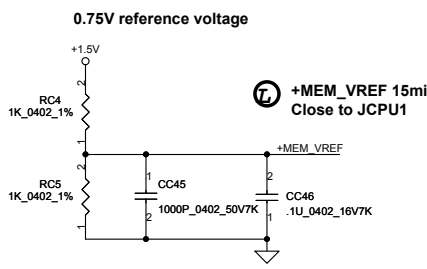
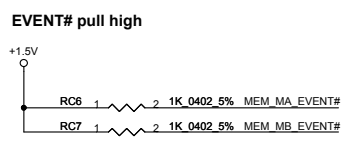
RC2 196_0402_1% P_ZVSS

P_ZVSS W/S=8/12 mil, <3000mil

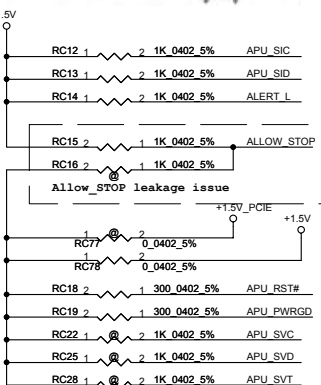
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Customer				Rev
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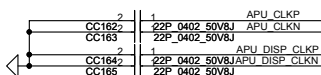
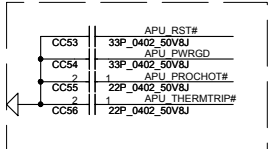
M_ZVDDIO W/S=8/12 mil, <1000mil



The diagram illustrates the system architecture. It consists of three main components: a System Processor, a VGA Transmitter, and a VGA Receiver. The System Processor is connected to the VGA Transmitter via SPI_TxData and to the VGA Receiver via SPI_Ack. The VGA Transmitter and Receiver are connected to each other via VGA_TxData and VGA_RxData. The VGA Transmitter and Receiver are also connected to a VGA Bus, which is connected to a VGA Display. The VGA Display is connected to a VGA Bus, which is connected to a VGA Display. The VGA Display is connected to a VGA Bus, which is connected to a VGA Display.

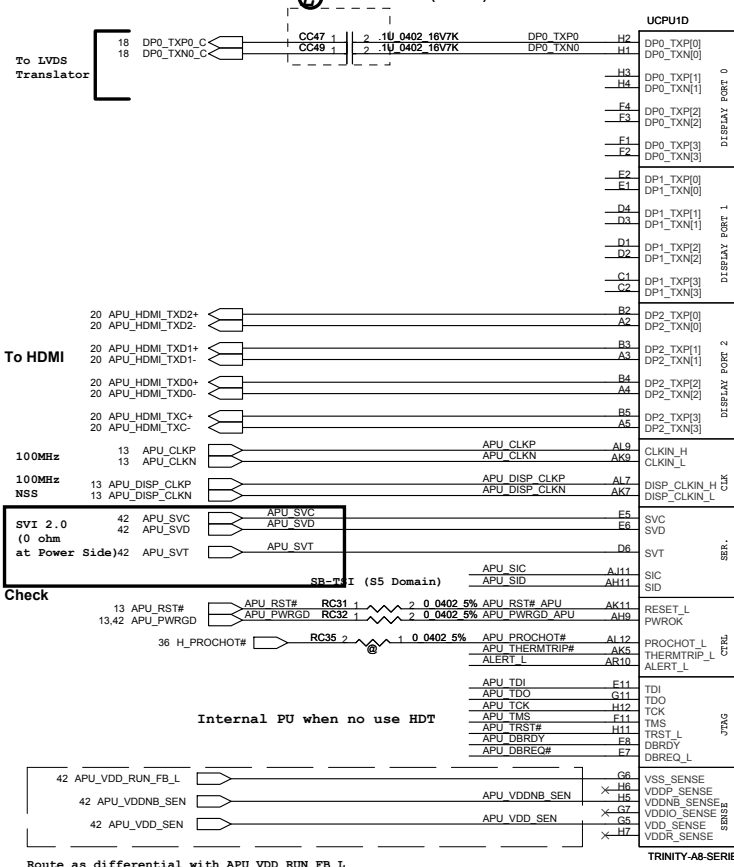


For ESD request close APU side



12/19 RF request

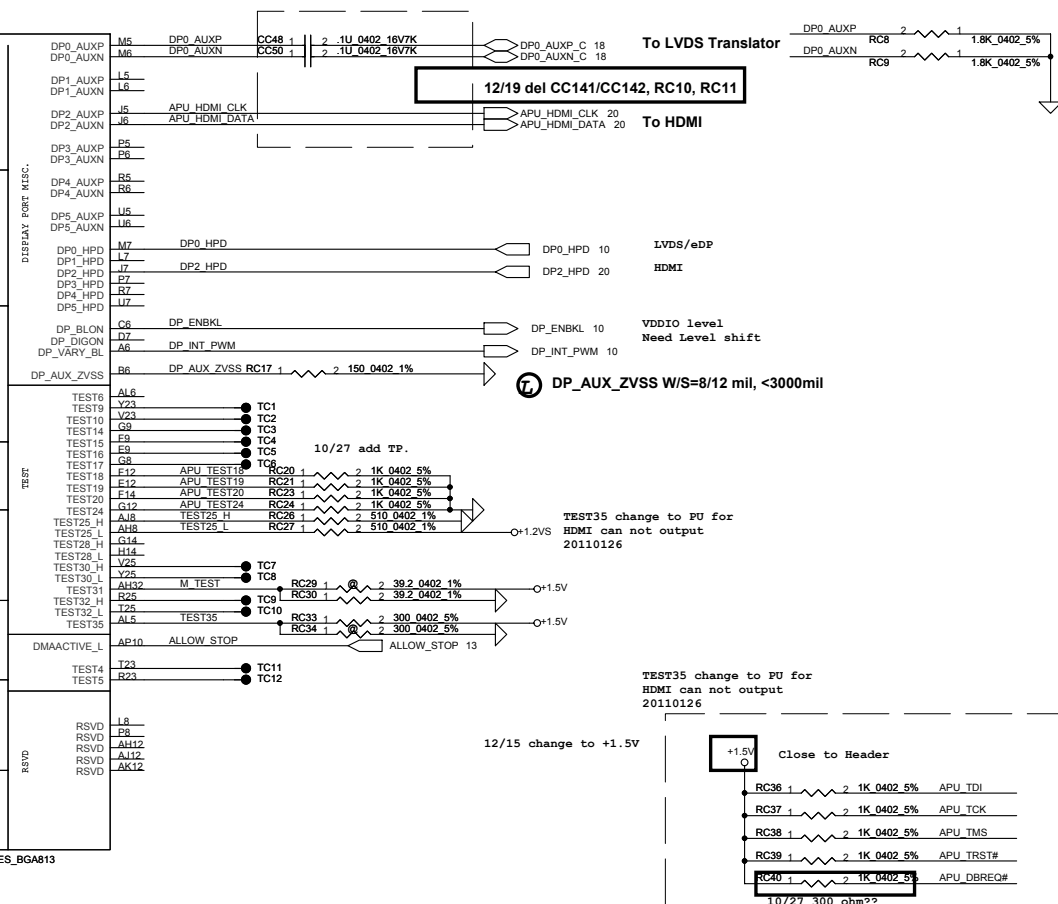
T Close to APU (JCPU1)



Route as differential with APU VDD RUN FB I

TRINITY-A8-SERIES BGA813

Place near APU



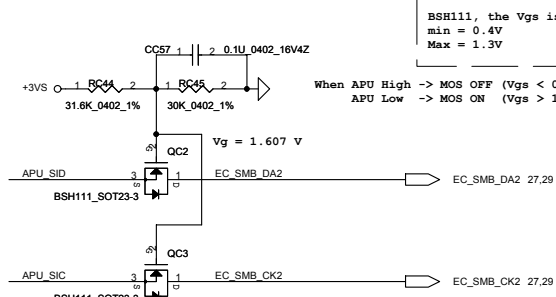
12/15 change to +1.5V

Close to Header

TEST35 change to PU for
HDMI can not output
20110126

12/19 remove damping 0ohm.

CPU TSI interface level shift



BSH111, the V_{gs} is:
min = 0.4V
Max = 1.3V

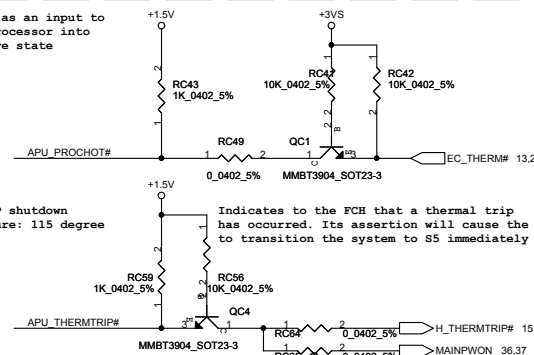
When APU High -> MOS OFF ($V_{gs} < 0.4V$)
 APU Low -> MOS ON ($V_{gs} > 1.3V$)

607 V

EC_SMB_DA2 27,29

EC SMB CK2 27.29

Asserted as an in
force processor
HTC-active state



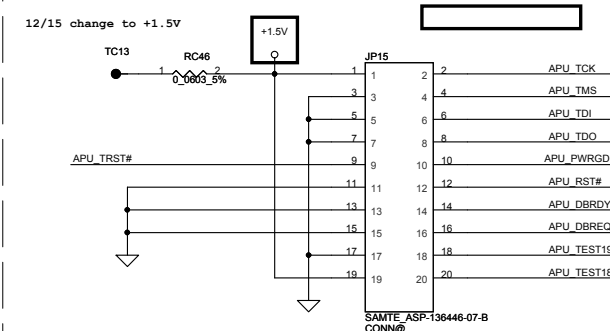
THERMTRIP shutdown
temperature: 115 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

W THERMTRIP# 15

MAINPWON 36 37

HDT Debug conn



SAMTE_ASP-136446-07-B
CONN@

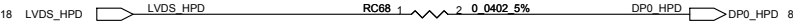
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HPD

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Translator and eDP HPD
From Translator or Conn.

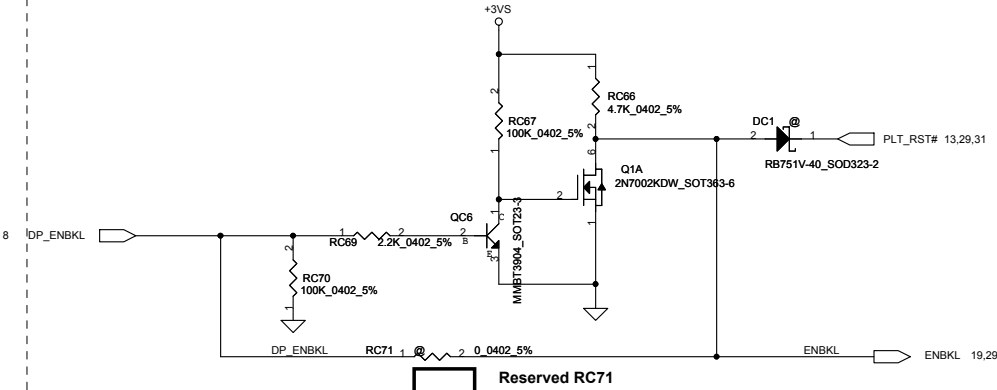


Del reserved NMOS

12/06 Del FCH_CRT_HPD



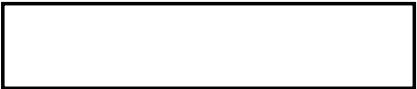
Panel ENBKL



Del VGA_ENBKL

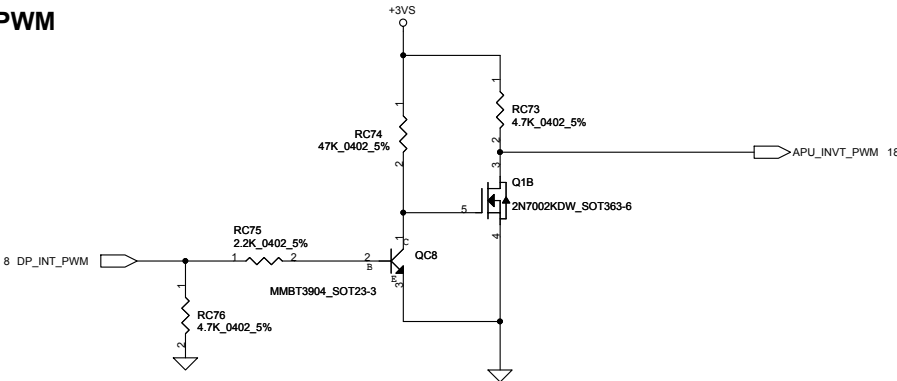


eDP Panel ENVDD





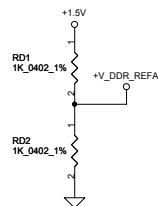
Del eDP panel control

Panel PWM



DDR3 SO-DIMM A

7 DDRA_SDQ[0..63] DDRA_SDQ[0..63]
7 DDRA_SDM[0..7]  DDRA_SDM[0..7]
7 DDRA_SMA[0..15]  DDRA_SMA[0..15]



100V 5000VA, 3.3V 6K

0.0025

100V 5000VA, 3.3V 6K

0.0025

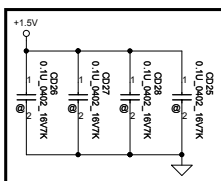
0.75V

0.0025

3.3V 6K

The schematic diagram illustrates a power supply circuit. It begins with a 1.5V input connected to a series of capacitors (CD12 to CD21) and resistors (G022, 330U, B2, 2.5V, R15M). A dashed box highlights the output section, which includes capacitors CD18, CD19, CD20, and CD21, and a resistor G022. The output is labeled SGA000004400.

DDR3 SO-DIMM A

[illegible]

DIMM A REV H:4mm

<Address: 00>

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		2011/06/29		Title	
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				Document Number	
				LA-8661P	
Date:		Tuesday, December 27, 2011		Sheet 11 of 47	

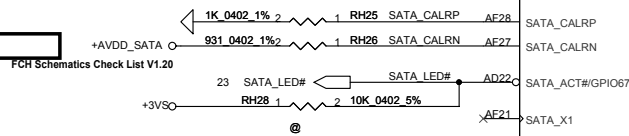
HDD1

22 SATA_STX_DRX_P0
22 SATA_STX_DRX_N0
22 SATA_DTX_SRX_N0
22 SATA_DTX_SRX_P0

SATA_STX_DRX_P0 AK19
SATA_STX_DRX_N0 AM19
SATA_DTX_SRX_N0 AL20
SATA_DTX_SRX_P0 AN20

12/12 del mSATA by customer

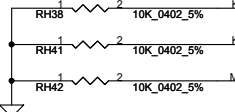
SATA_CALRP=35ohm,<1000mi
SATA_CALRN=35ohm,<1000mi



Del WL_OFF#_2

21 BT_ON#
21 WL_OFF#

BT_ON#
WL_OFF#



UH1B
SATA_TX0P
SATA_TX0N
SATA_RX0N
SATA_RX0P
SATA_TX1P
SATA_TX1N
SATA_RX1N
SATA_RX1P
SATA_TX2P
SATA_TX2N
SATA_RX2N
SATA_RX2P
SATA_TX3P
SATA_TX3N
SATA_RX3N
SATA_RX3P
SATA_TX4P
SATA_TX4N
SATA_RX4N
SATA_RX4P
SATA_TX5N
SATA_RX5N
SATA_RX5P
NC8
NC7
NC8
NC9
NC10
NC11
NC12
NC13
SATA_CALRP
SATA_CALRN
SATA_LED#
SATA_ACT#
SATA_X1
SATA_X2
FANOUT0/GPIO52
FANOUT1/GPIO53
FANOUT2/GPIO54
FANIN0/GPIO56
FANIN1/GPIO57
FANIN2/GPIO58
TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174

HUDSON-2

SD_CLK/CLK_2/GPIO73
SD_CMD/SLD_2/GPIO74
SD_CD/GPIO75
SD_WP/GPIO76
SD_DATA0/SDAT0_2/GPIO77
SD_DATA1/SDAT0_2/GPIO78
SD_DATA2/GPIO79
SD_DATA3/GPIO80

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTLRXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTLTXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

SPI_DI/GPIO164
SPI_DO/GPIO163
SPI_CLK/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/SPI_WP#/GPIO161

VGA_RED
VGA_GREEN
VGA_BLUE
VGA_HSYNCGP068
VGA_VSYNCGP069
VGA_DDC_SDA/GP070
VGA_DDC_SCL/GP071

VGA_DAC
VGA_DAC_RSET
AUX_VGA_CH_P
AUX_VGA_CH_N
AUXCAL

ML_VGA_L0P
ML_VGA_L0N
ML_VGA_L1P
ML_VGA_L1N
ML_VGA_L2P
ML_VGA_L2N
ML_VGA_L3P
ML_VGA_L3N

ML_VGA_HPD/GPIO229

VIN0/GPIO175
VIN1/GPIO176
VIN2/SDAT1_1/GPIO177
VIN3/SDAT0_1/GPIO178
VIN4/SLOAD_1/GPIO179
VIN5/SCLK_1/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182

NC1
NC2
NC3
NC4
NC5

AL14
AN14
AH12
AH13
AK13
AM13
AH15
AL15

AC4
AD3
AD3
W10
AB8
AH7
AE7
AD7
AG8
AD1
AB7
AF9
AG6
AG3
AD8
AB9
AC2
W9

V6
V6
V3
T6
V1

L30
L32
M29
M28
N30
M33
N32

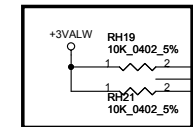
K31
V28
V29
U28
T31
T33
T29
T28
R32
R40
P29
P28

C29

N2
M3
L2
N4
P1
P3
M1
M5

RH32
RH33
RH34
RH35
RH36
RH37
RH38
RH40

AG16
AH10
AG27
L4

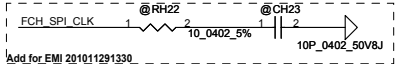


Check CS# PU R 1k or 10k and pop/nopop
SCL v1.20 : If an SPI ROM is shared between
the FCH and the Embedded Controller
a 10-K pull-up resistor to +3.3V_S5 is installed.

4MB SPI ROM
& Non-share ROM.

UH3
CS#
SO/IO1
WP#
GND
VCC
HOLD#
SCLK
SI/SIO0

FCH_SPI_CS1#
FCH_SPI_MISO
FCH_SPI_WP#
FCH_SPI_VCC
FCH_SPI_HOLD#
FCH_SPI_CLK
FCH_SPI_MOSI



Add for EMI 201011291330

GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-K 5% resistor.
FCH SCL v1.20 #19-85

GBE_PHY_INTR

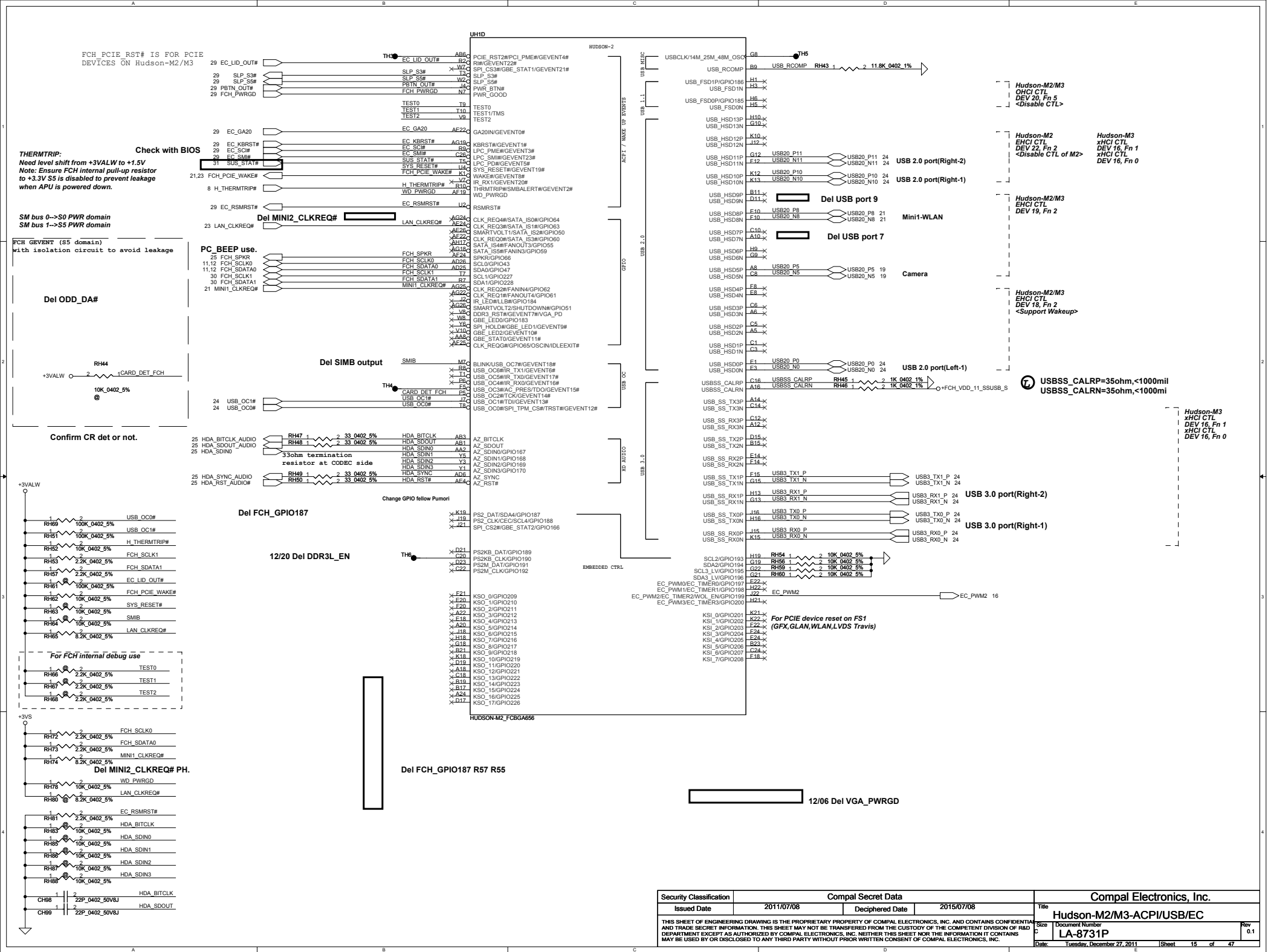
Removed RGMII/MII support and updated termination
requirements for GBE_COL, GBE_CRS, GBE_RXERR
and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20

12/19 remove RH29, RH31 for HW request

Check?

Confirm BT_ON# or BT_ON
Del W_DISABLE#_2

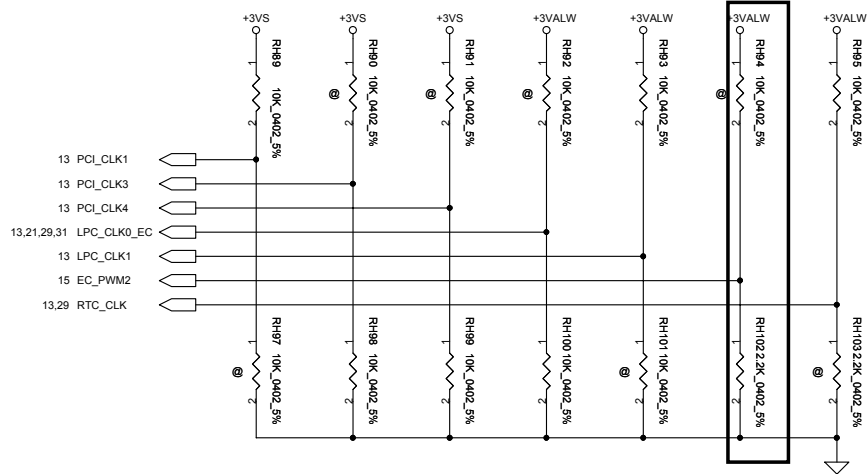




STRAP PINS

Change to SPI

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



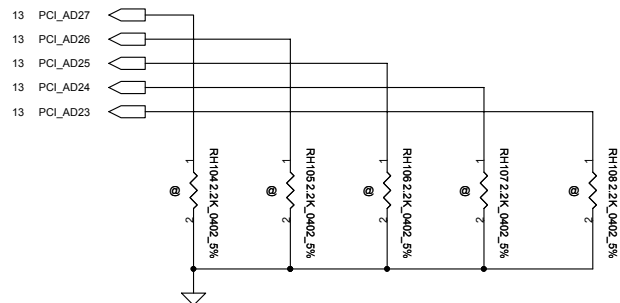
Remove VGA_PD

Remove VGA_PD

DEBUG STRAPS

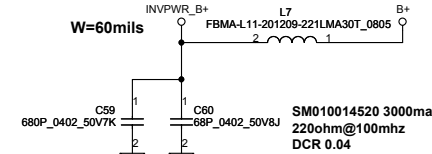
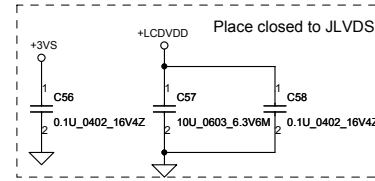
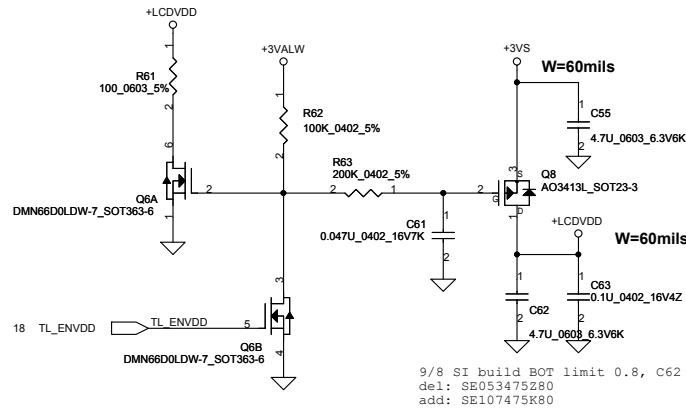
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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Customer				Document Number	Rev
Date: Tuesday, December 27, 2011				LA-8731P	0.1
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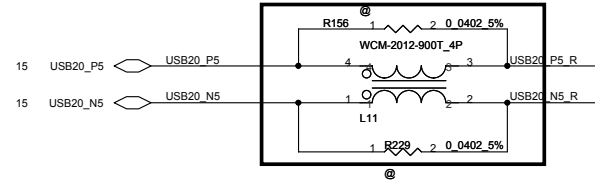
LCD POWER CIRCUIT



LCD/LED PANEL Conn.

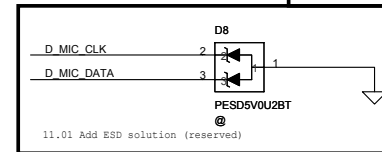
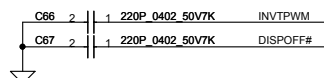
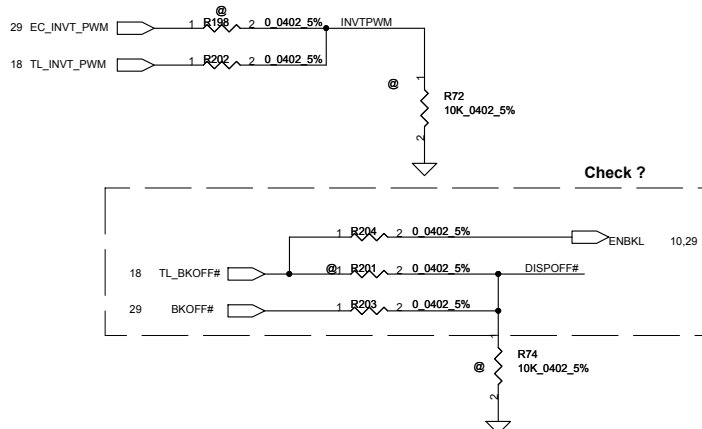
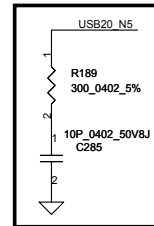
W=60mils W=60mils

Check pin definition.

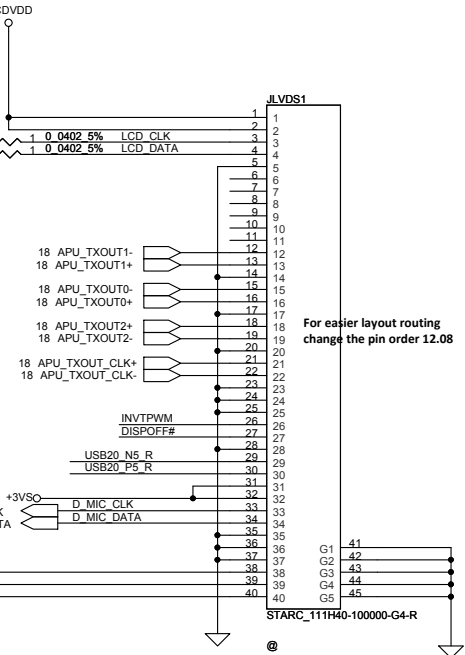


8/19 change stuff L26 by EMI request

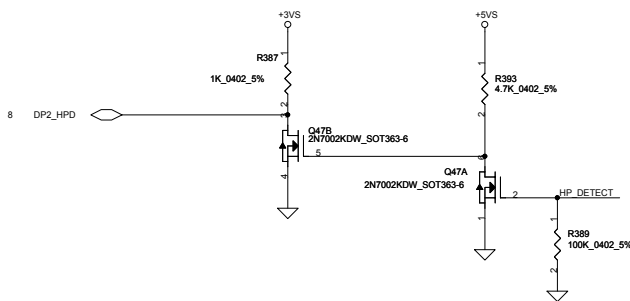
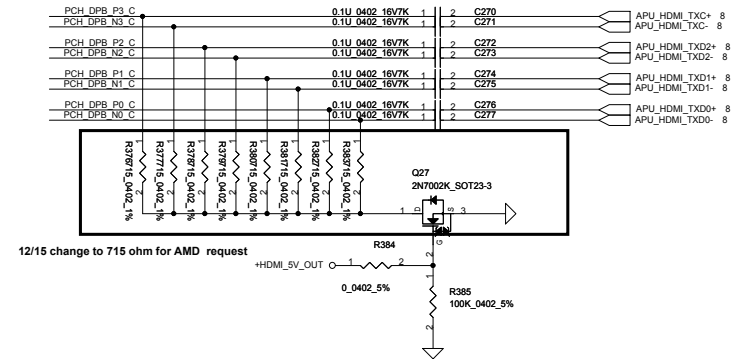
12/21 for AMD issue workaround



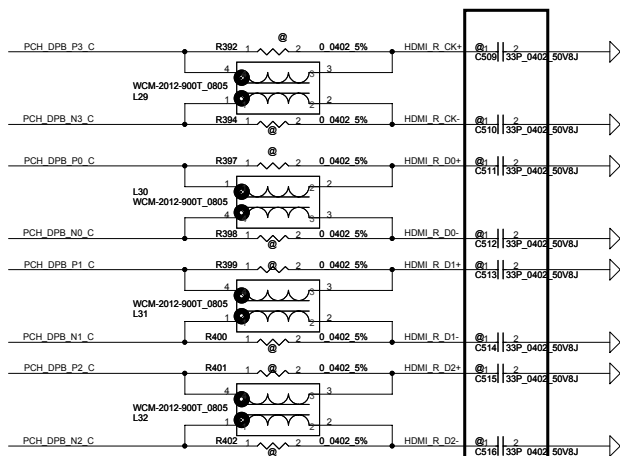
Check



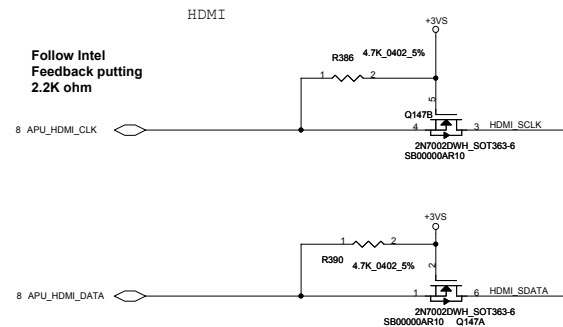
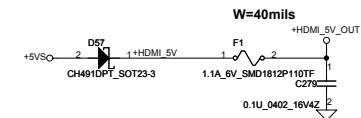
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Issued Date		Deciphered Date		Document Number	
2011/06/29		2011/06/29		LA-8731P	
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Sheet		19		of 47	



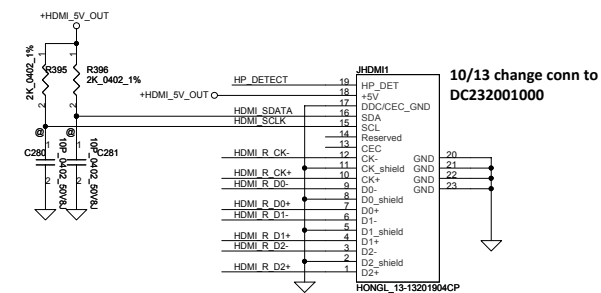
SM070001310 400ma 90ohm@100mhz DCR 0.3

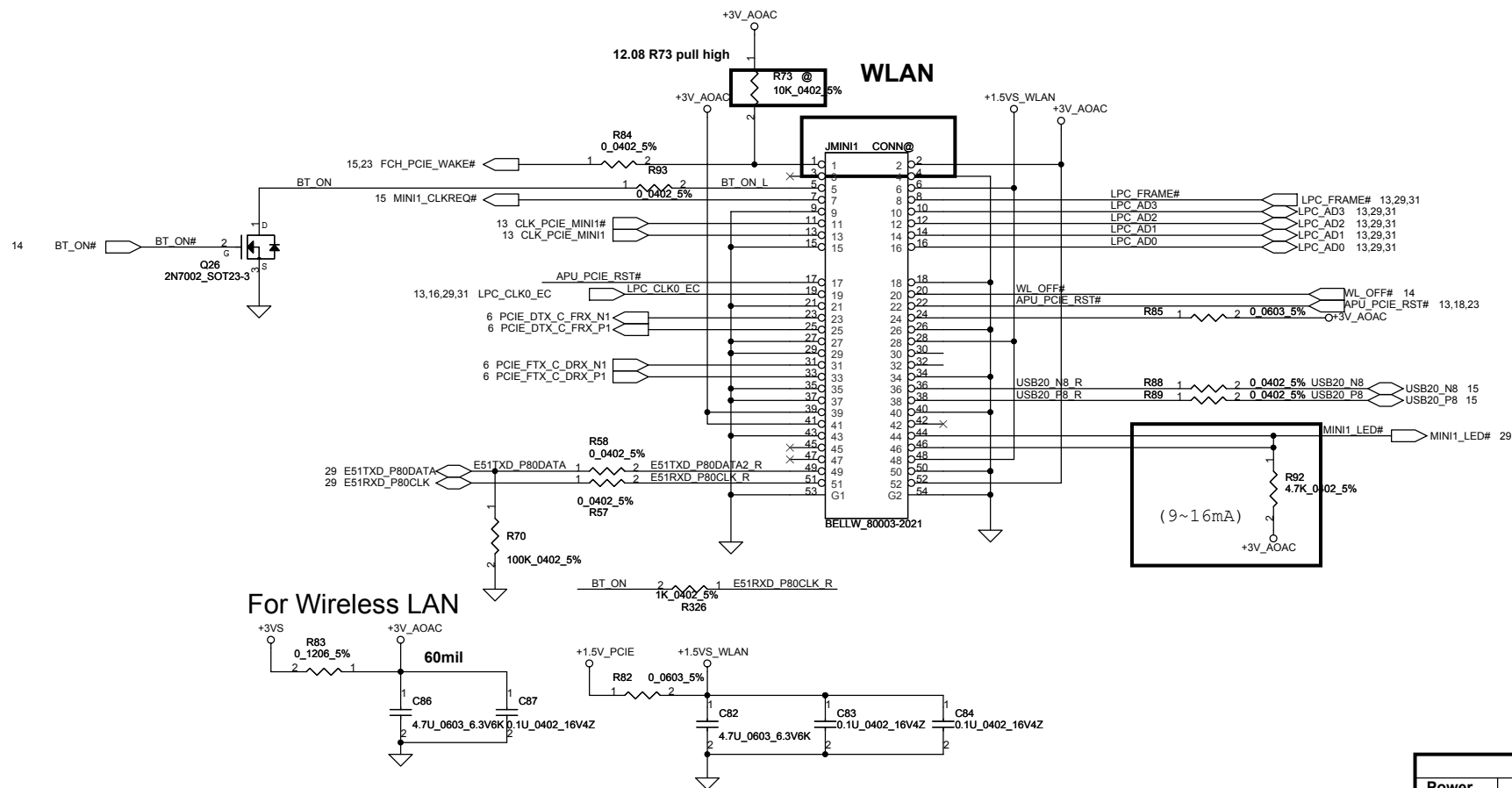


Follow EMI request add 33pF cap to GND.
11.02

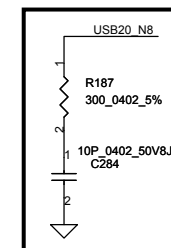


5V PULL UP IN CONNECTOR SIDE





12/21 for AMD issue workaround



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

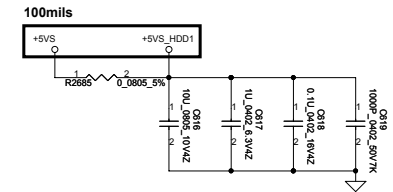
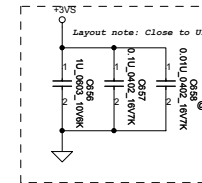
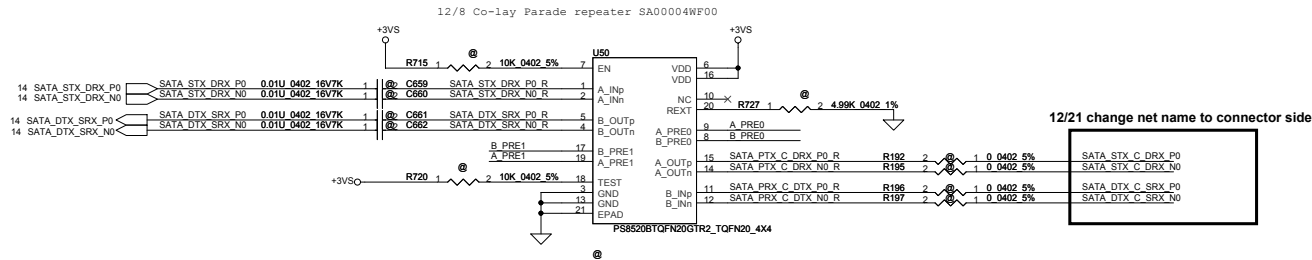
11/23 Del AOAC

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				Sheet	21 of 47
				Rev	0.1

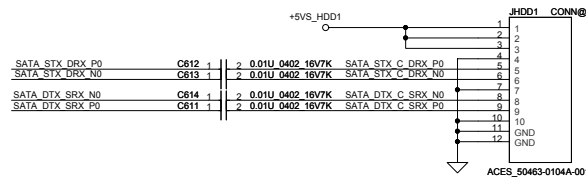
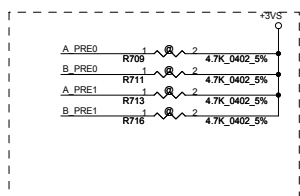
mSATA Conn.

12/12 Del mSATA by customer

SATA Redriver



Note: Add EQ pin for STA1102RQTR

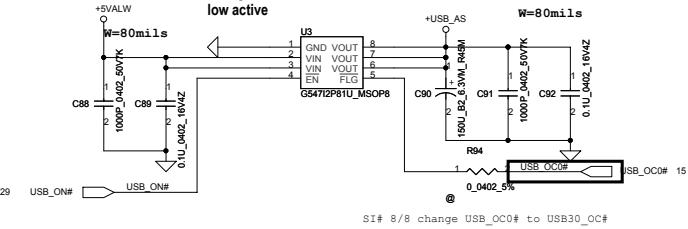


SATA connector

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				Sheet	22 of 47

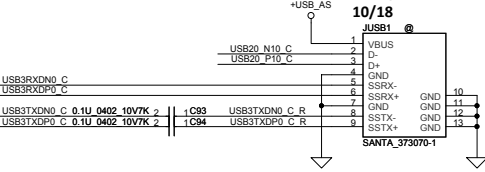
USB3.0

USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

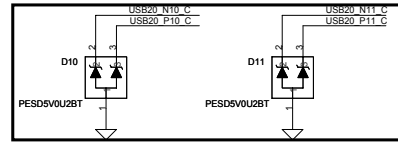


SI# 8/8 change USB_OC# to USB30_OC#

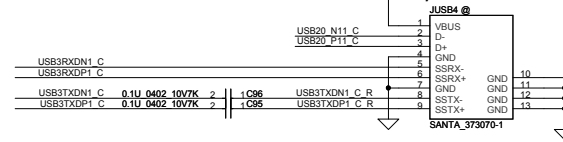
Change conn to SANTA-373070



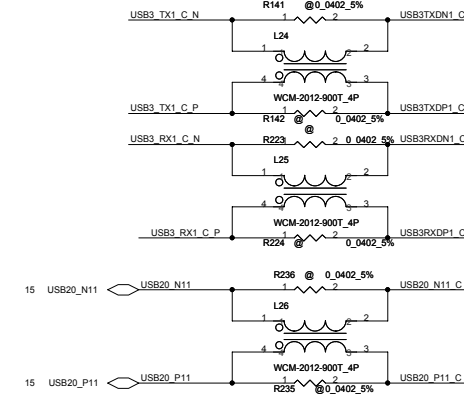
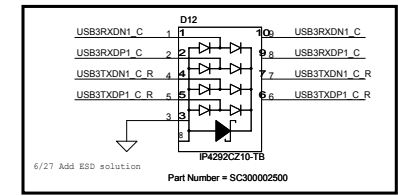
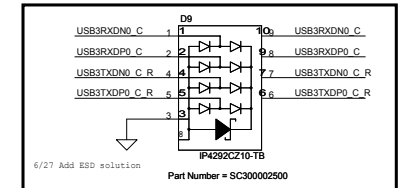
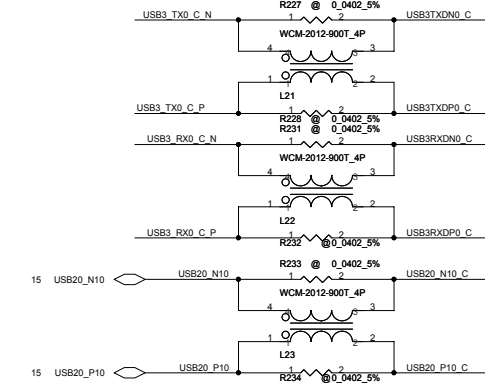
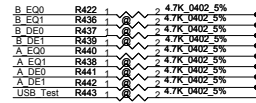
Change P/N from SCA00000T00 to SCA00001L00
11.01



Change conn to SANTA-373070
10/18



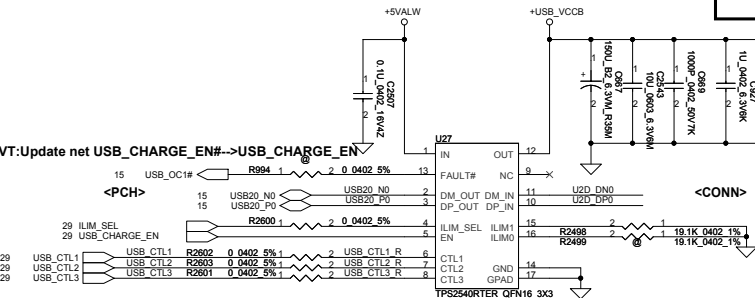
Programable output pre-emphasis level setting for
channel A1&A2, B1&B2
3.3V tolerant. Internally pulled down at ~150KΩ
[A_DE1, A_DE0] [B_DE1, B_DE0] == ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5.0dB de-emphasis



USB2.0 & charger

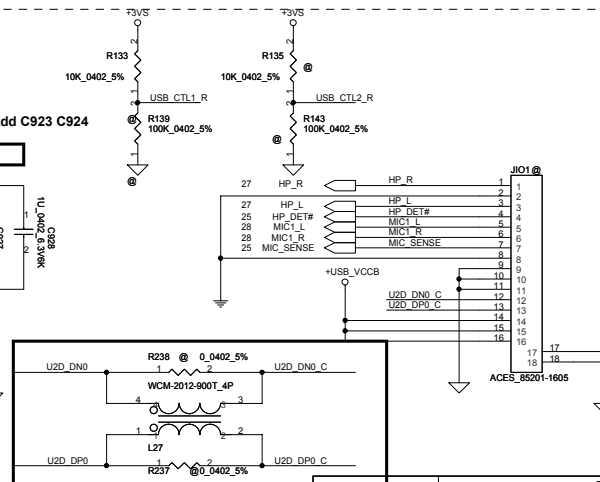
USB charger footprint need change to TPS2543
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)

Pre MP:Add C923 C924

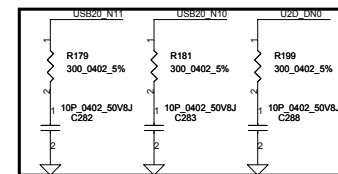


PVT:Remove R2664 R2499 R2500 R2501 for DFX issue

Follow EMI request add choke
11.08



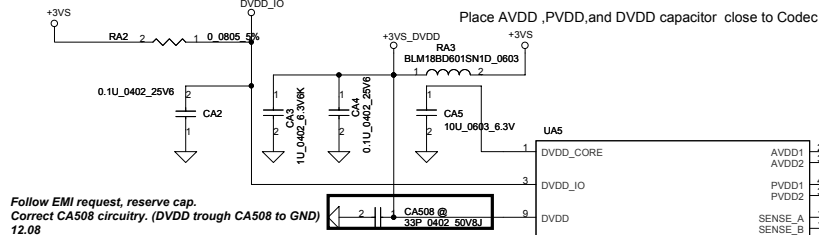
12/21 for AMD issue workaround



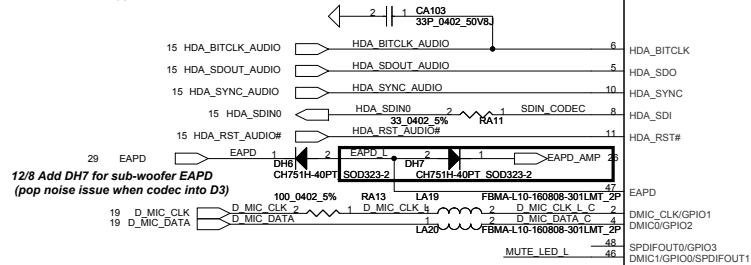
Check mode with customer?

State	S0	S3, S4, S5
Mode	CDP	DCP
Control pin	CTL1 CTL2 CTL3 ILIM_SEL	CTL1 CTL2 CTL3 ILIM_SEL
	1 1 1 1	0 0 1 1

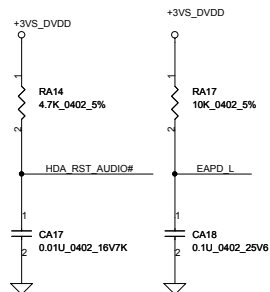
DVDD_IO should match with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)



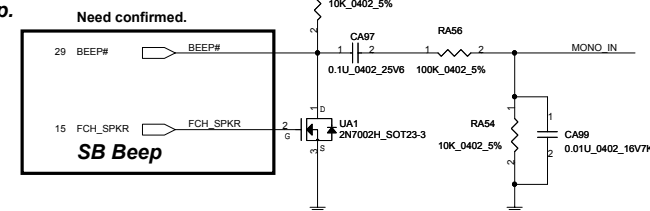
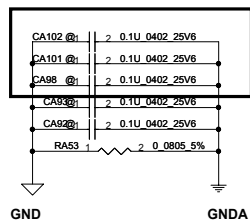
Follow EMI request, reserve cap.
Correct CA508 circuitry. (DVDD trough CA508 to GND)
12.08



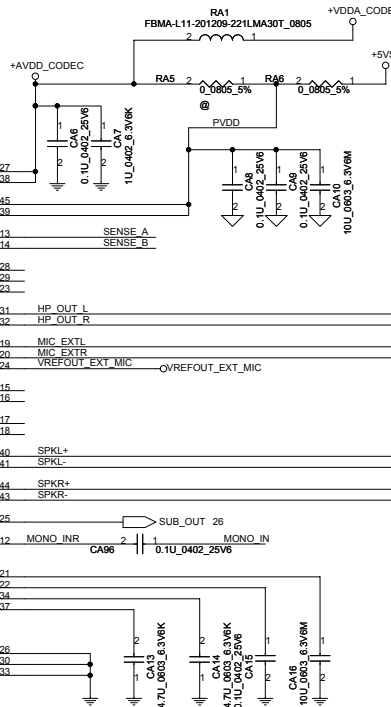
12/8 Add DH7 for sub-woofer EAPD
(pop noise issue when codec into D3)



Follow EMI request, reserve cap.
11.03

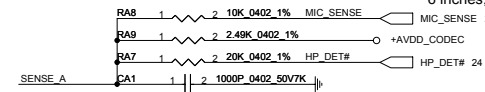


Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

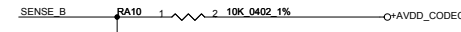


Place C209, C210, CA87, CA89 close to Codec

PLACE CLOSE TO U1 PIN 13



If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF



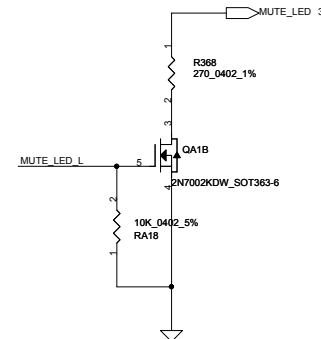
PLACE CLOSE TO U1 PIN 14

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

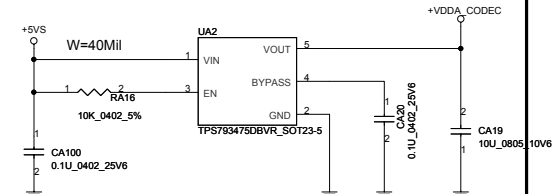
HP Jack

Ext MIC

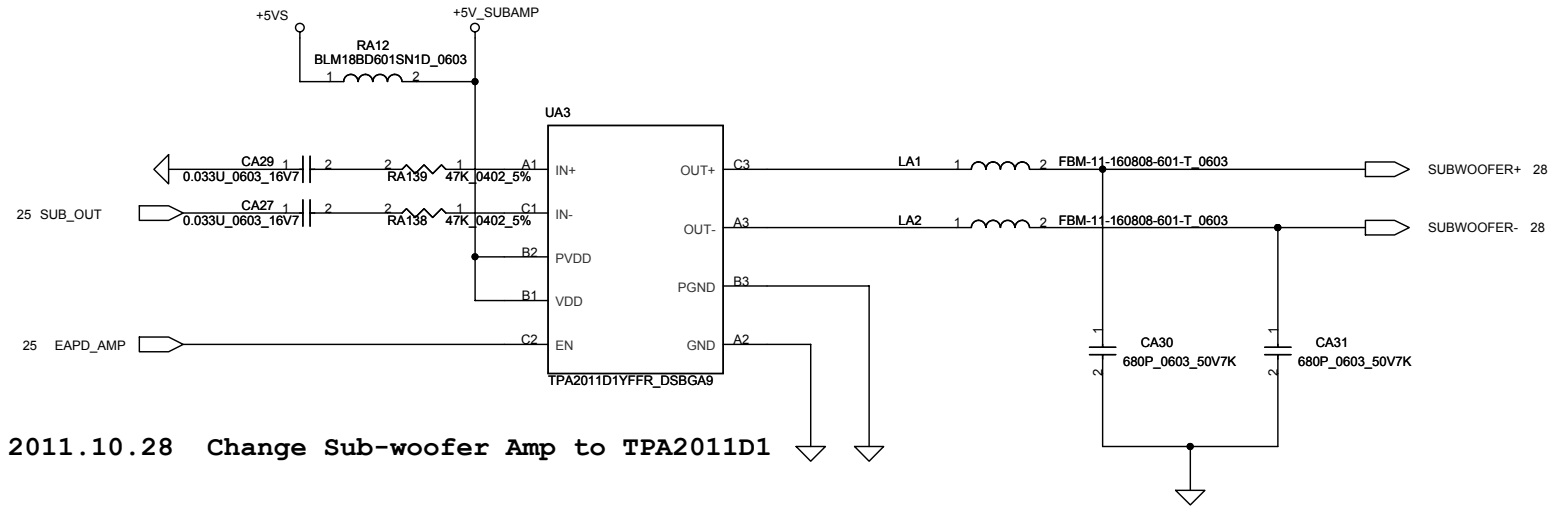
Internal SPKR(front stereo speaker)



9/27 LDO TPS793475DBVR for audio power



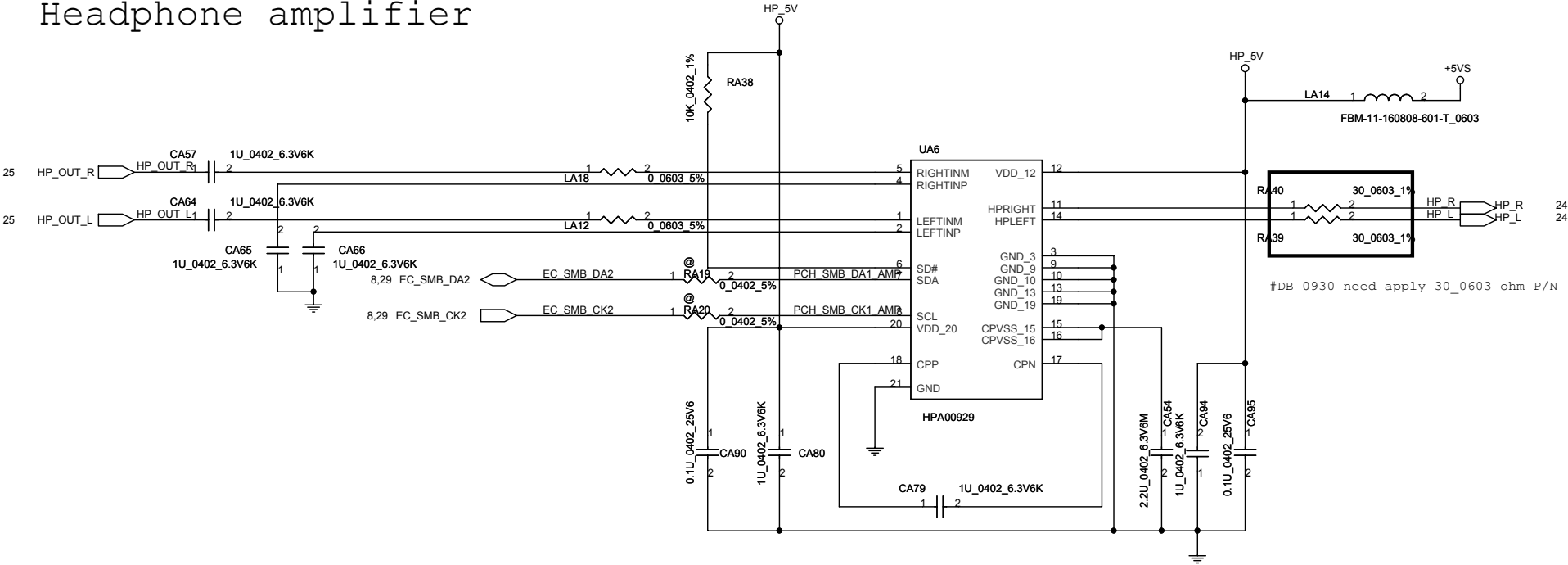
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Audio IDT 92HD91	
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Date:	Tuesday, December 27, 2011	Sheet	25	of 47	



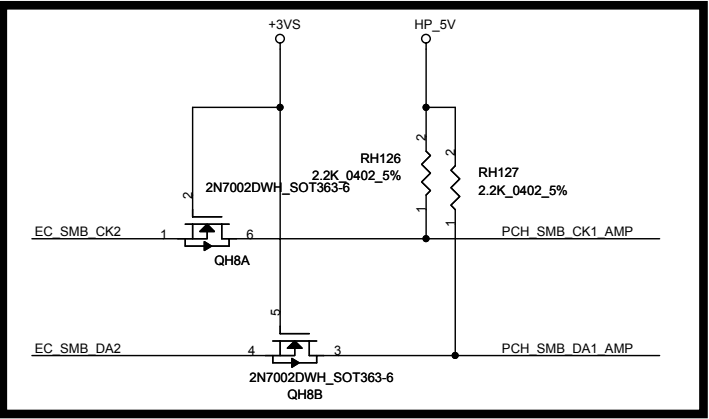
2011.10.28 Change Sub-woofer Amp to TPA2011D1

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				Date:	Tuesday, December 27, 2011
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Headphone amplifier

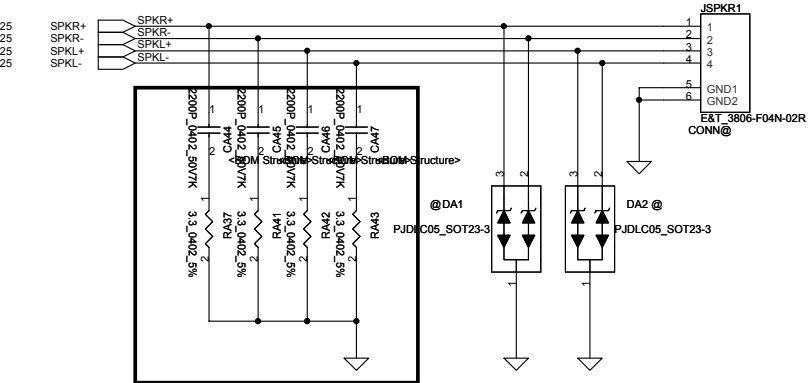


Add level shift 11.06



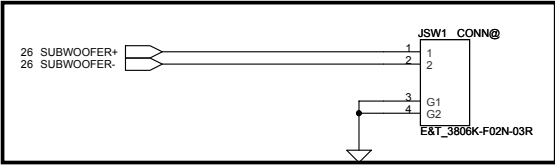
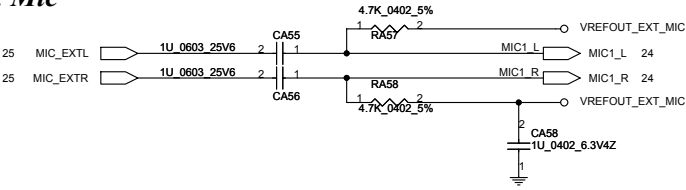
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Audio SPK/HP Amplifier
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				Rev	0.1
				Date:	Tuesday, December 27, 2011
				Sheet	27 of 47

Front Speaker Connector 1



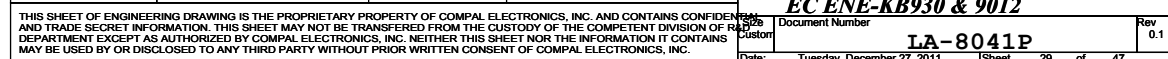
Need place rear Audio Codec (UA5)

Ext. Mic



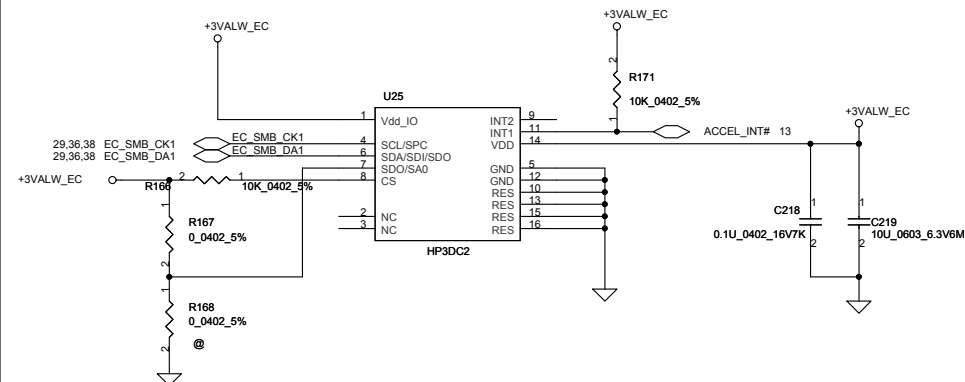
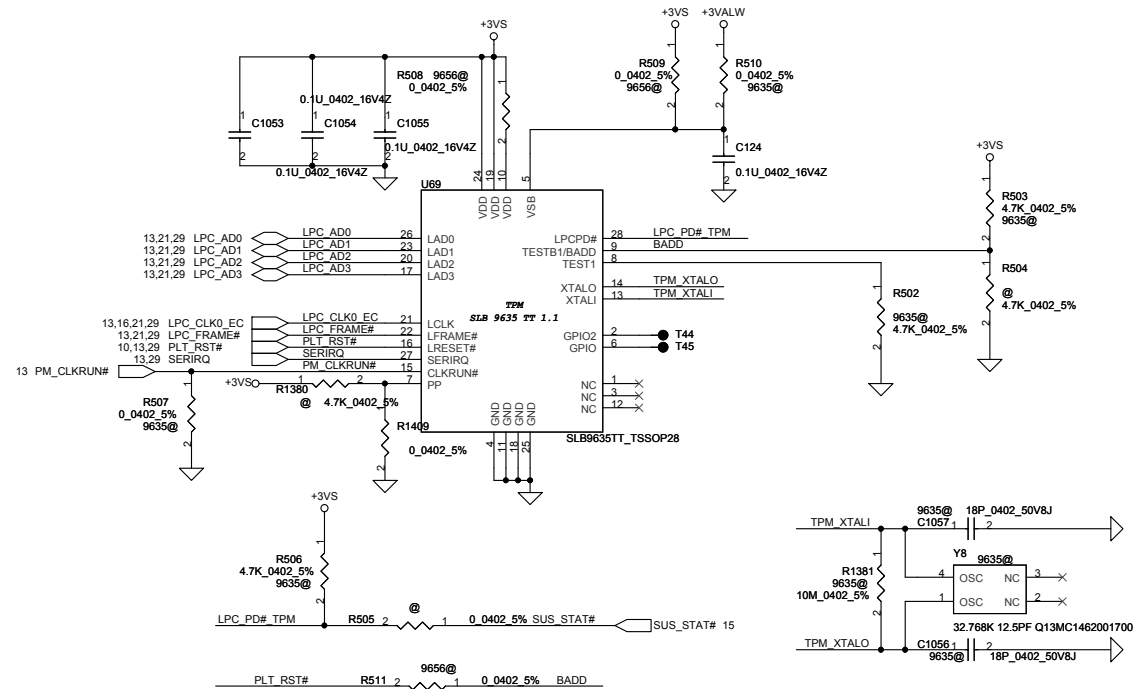
Change 4pins to 2 pins
12.13

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2009/04/07	Deciphered Date	2012/10/21	
Title		Audio SPK Conn/Jack/MIC		Size	
Document Number		LA-8731P		Rev	
Date:		Tuesday, December 27, 2011		Sheet	
28		of		47	
0.1					

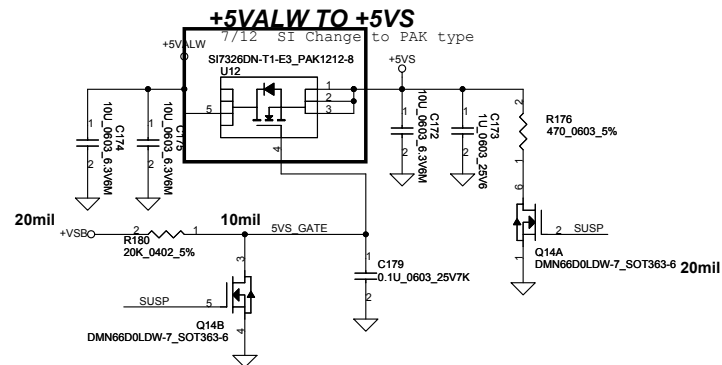


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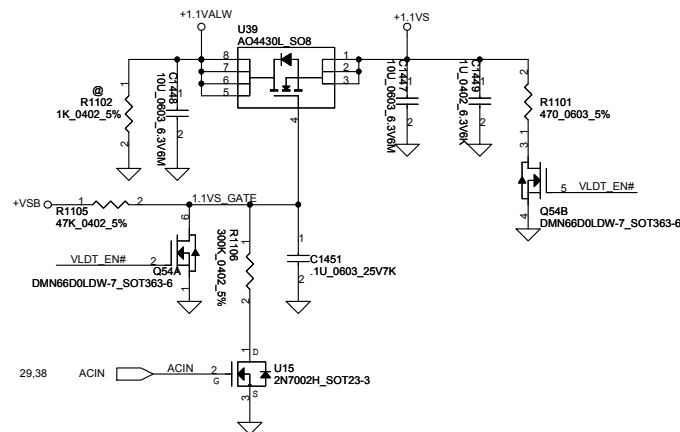
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***TPM1.2***

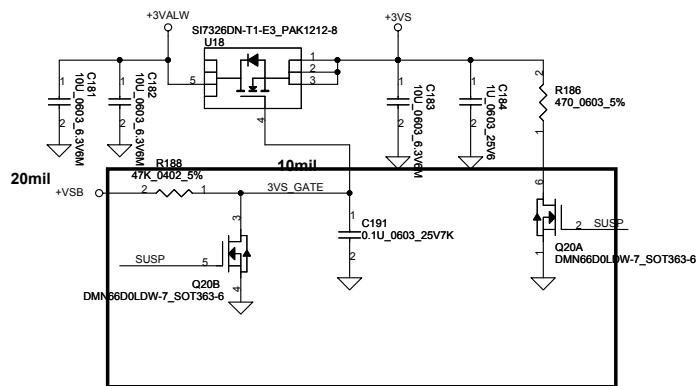
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	Title	TPM/Gsensor
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				LA-8731P	
Date:	Tuesday, December 27, 2011	Sheet	31	of	47



+1.1VALW TO +1.1VS (1.1A)

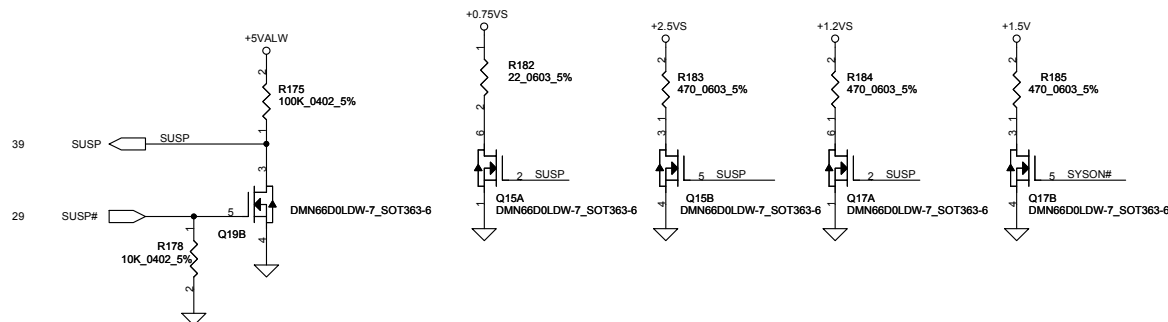
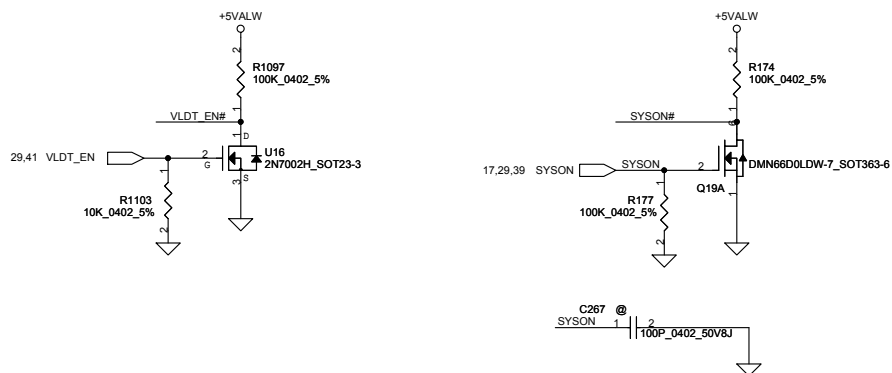
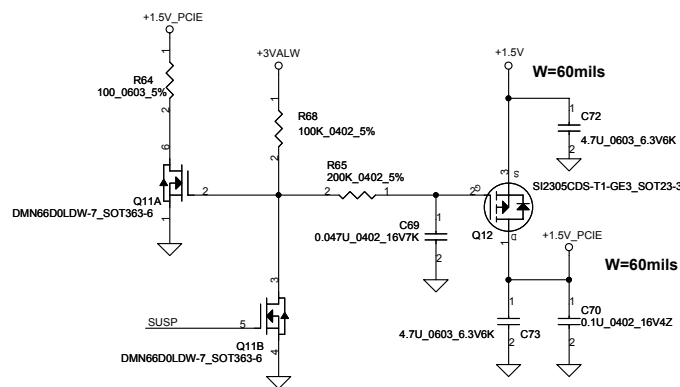


+3VALW TO +3VS

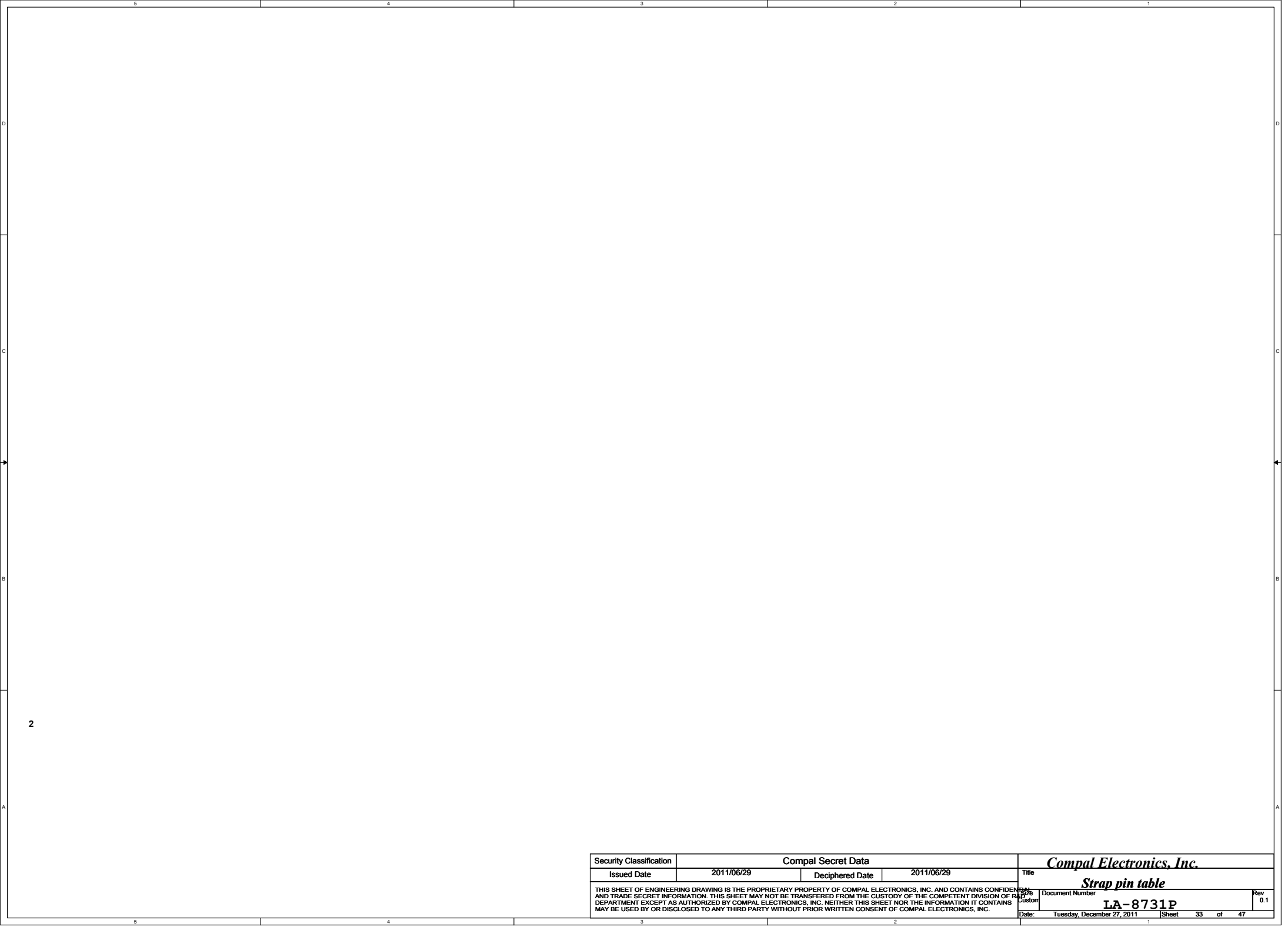


6/24 Q20 and Q21 to Q20 change to Dule mos package

+1.5VTO +1.5V_PCIE

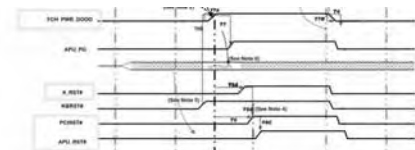
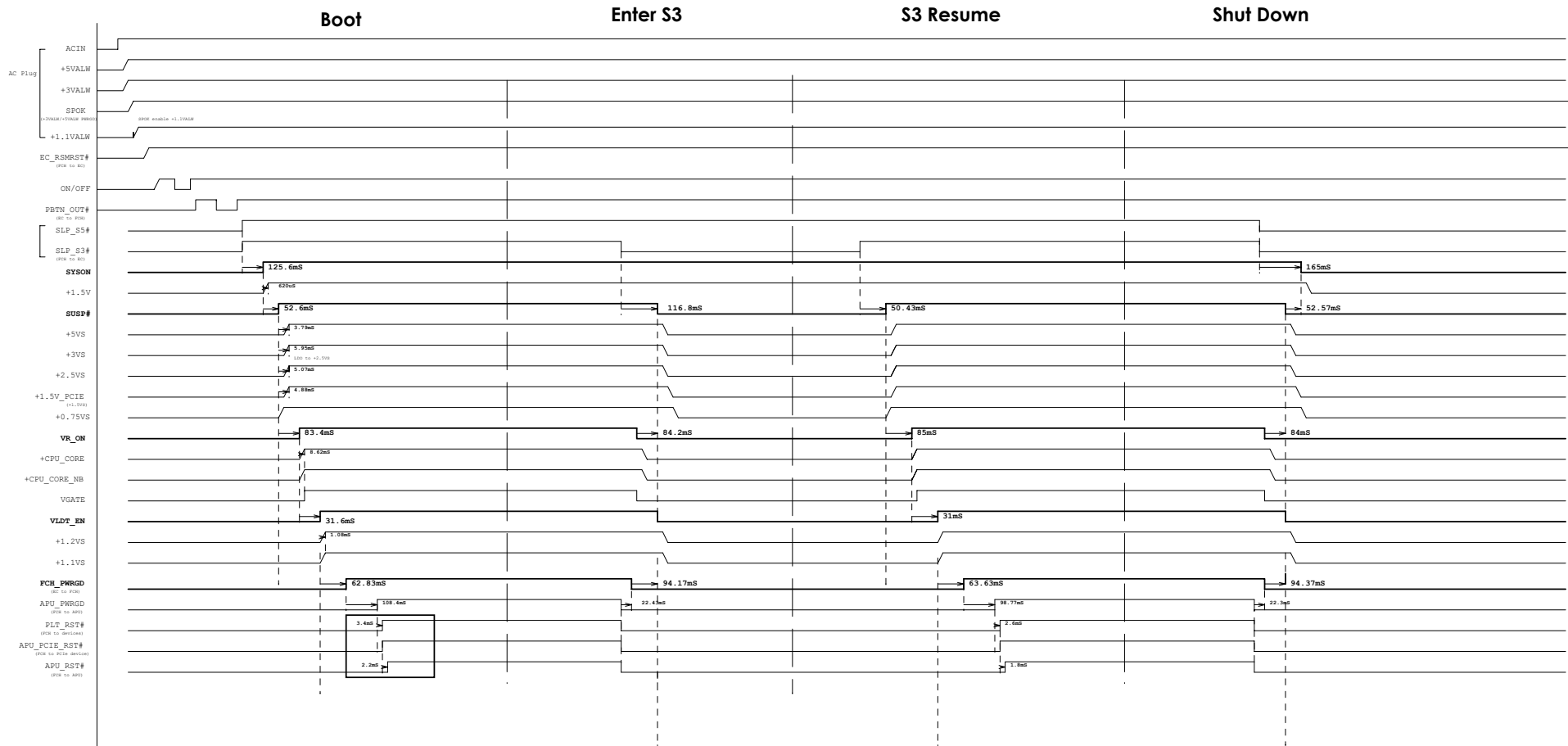


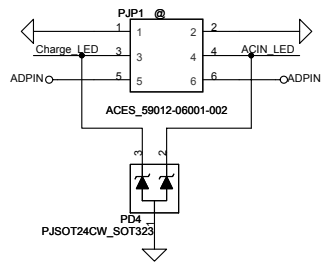
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Issued Date			Deciphered Date		Title	
2011/06/29			2011/06/29		DC Interface	
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			Date:		Tuesday, December 27, 2011	
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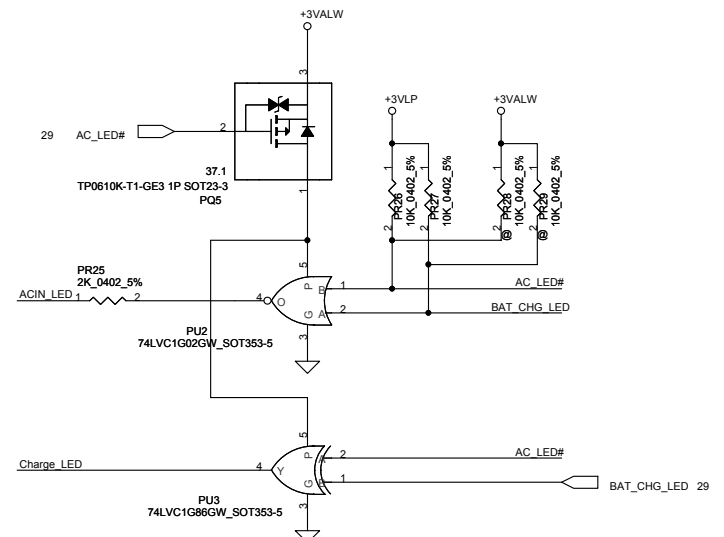
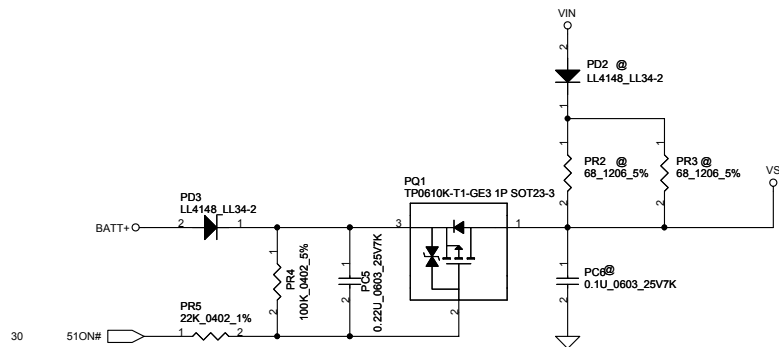
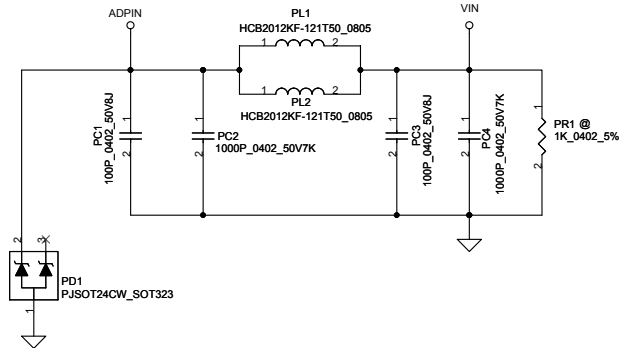
2

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Strap pin table	
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				0.1	LA-8731P	0.1
				Date:	Tuesday, December 27, 2011	Sheet 33 of 47

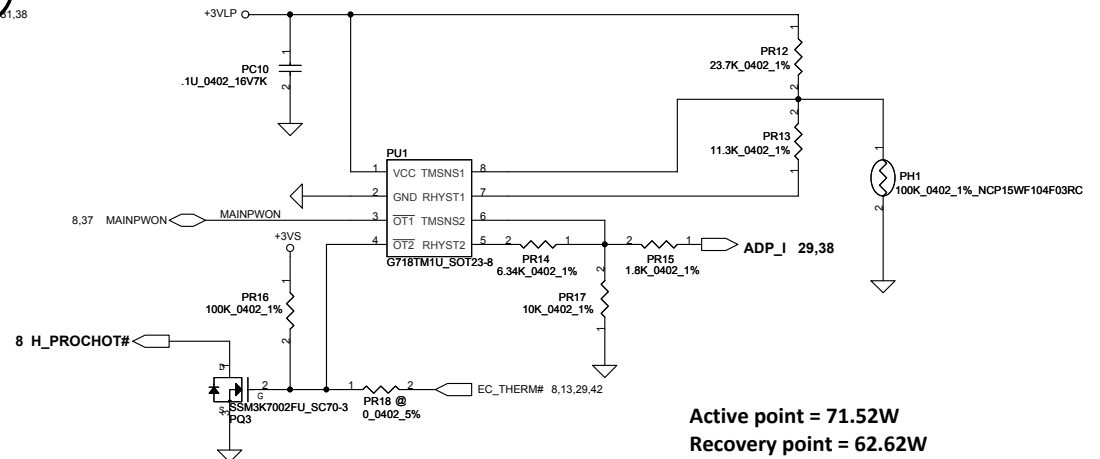
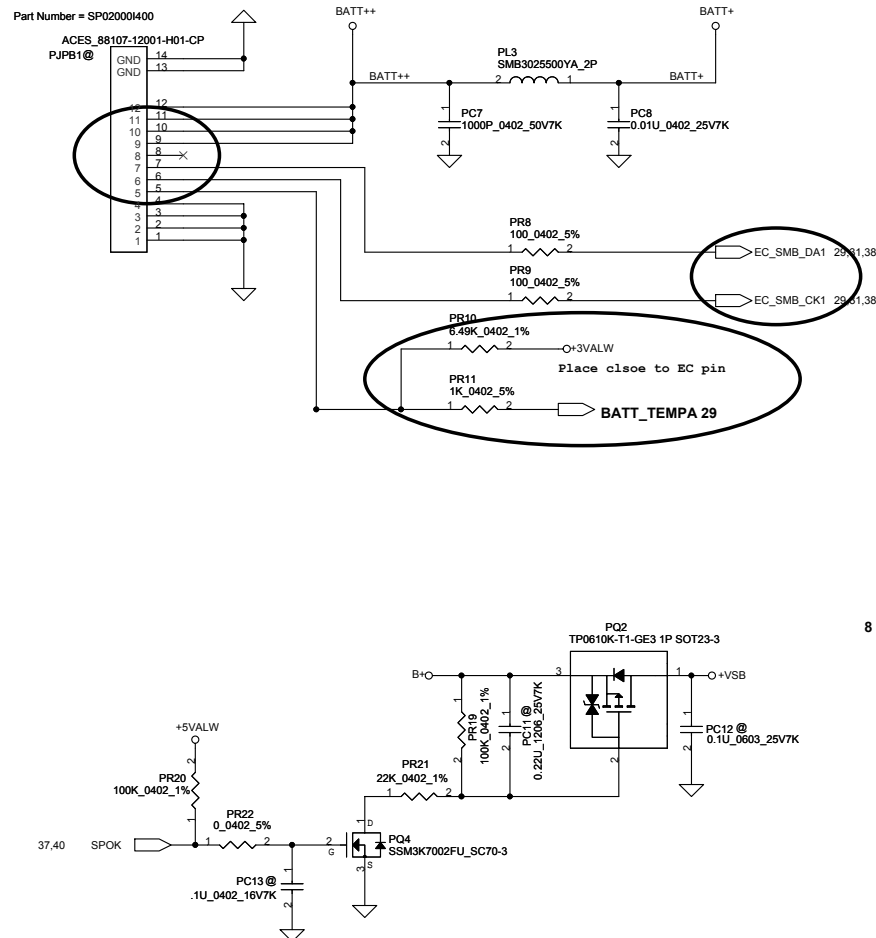




ESD diode : SCA00001G00



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)



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				LA8712P
				Rev 0.1
				Date: Tuesday, December 27, 2011
				Sheet 36 of 46

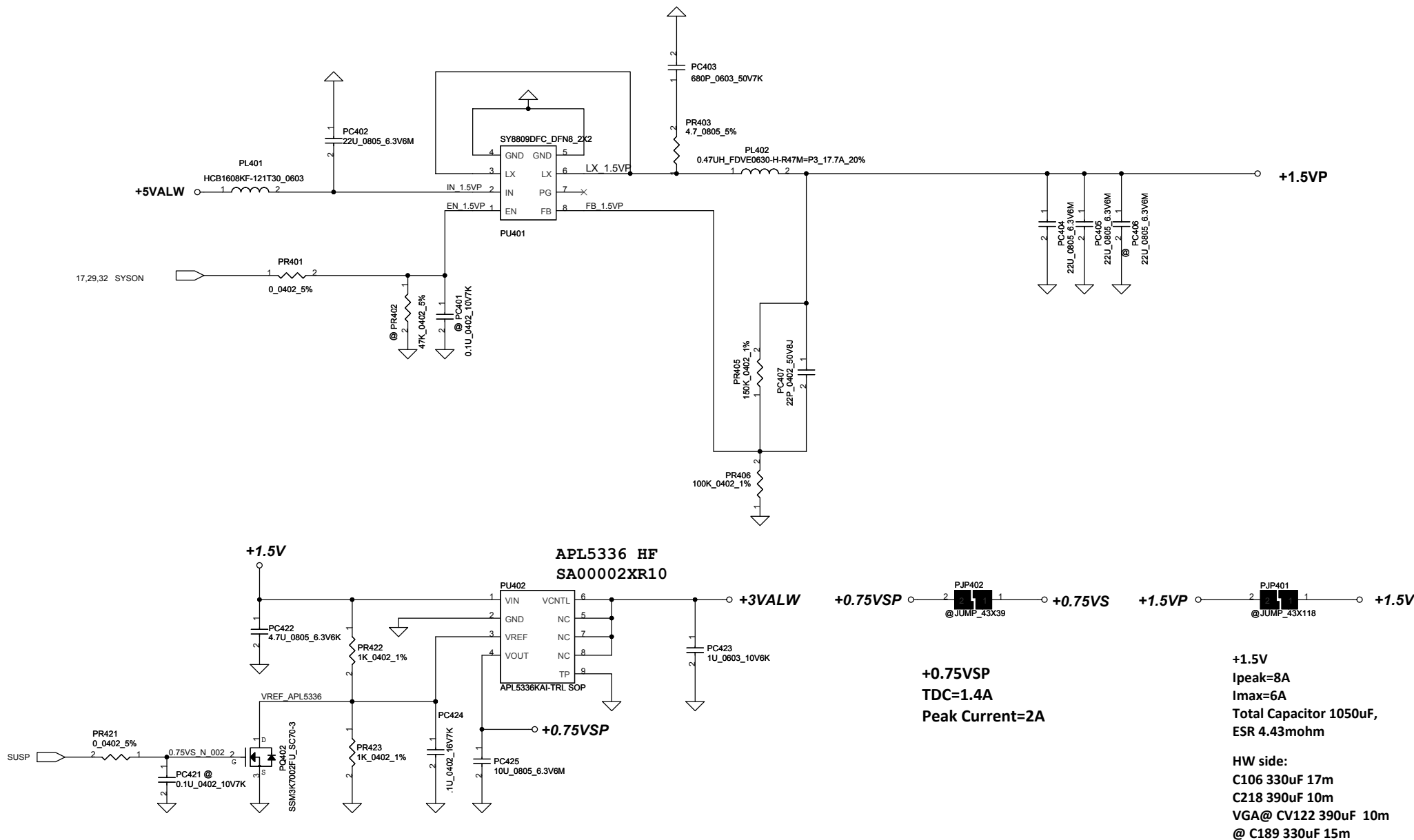
2011/03/18
delete VIN voltage
detecting circuit

Vin Detector

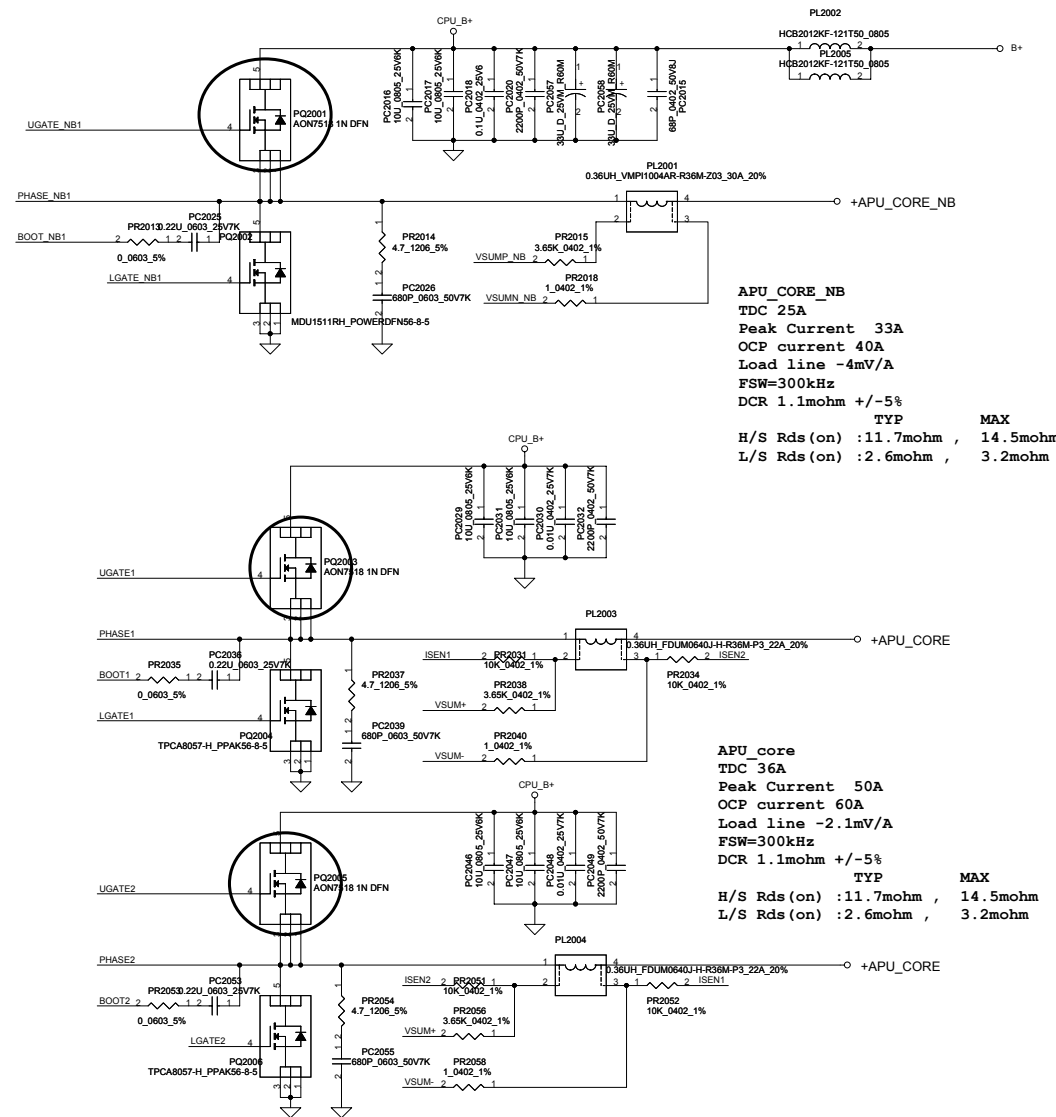
Min.	Typ	Max.
	17.33V	
	16.98V	

ILIM and external DPM
4.36A

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				LA-8712P	0.1
Date:		Tuesday, December 27, 2011		Sheet	38 of 46

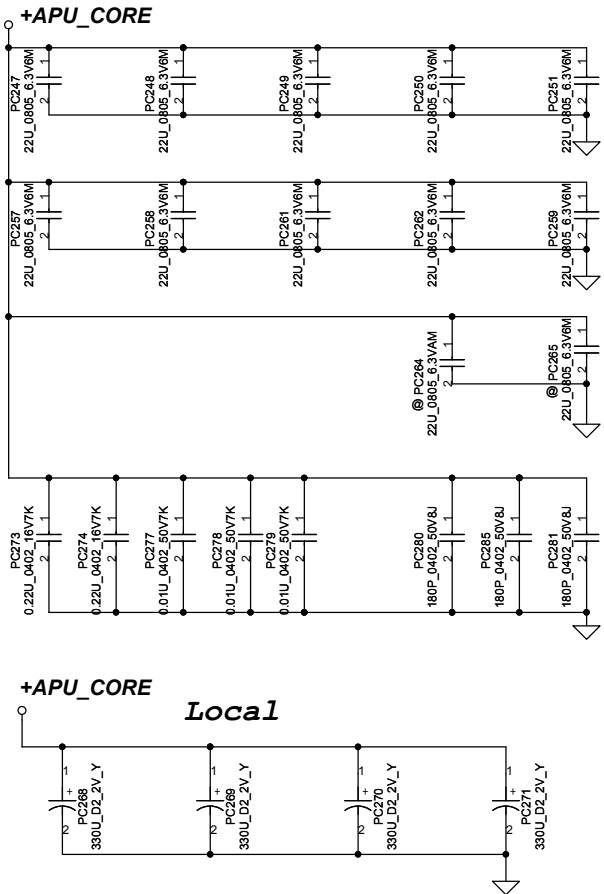


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				Tuesday, December 27, 2011	39 of 46

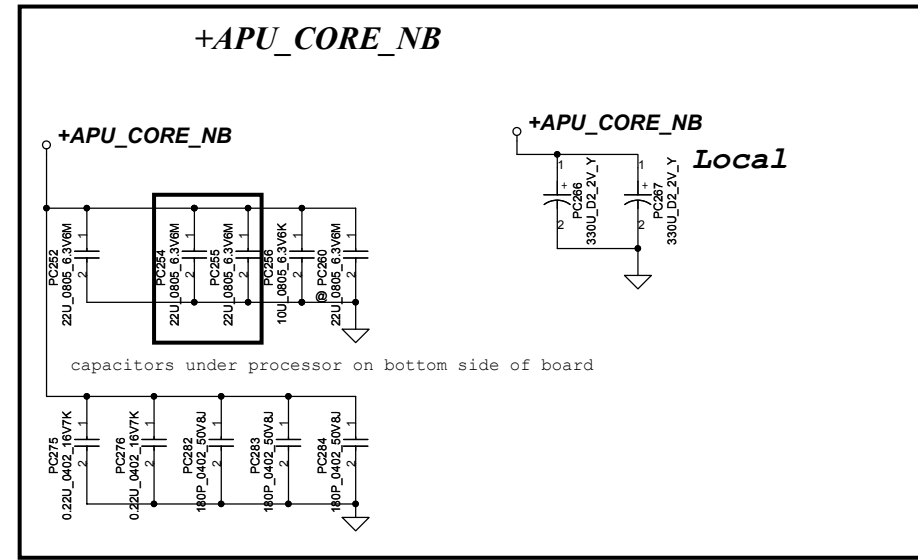


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			Date	Thursday, December 27, 2011	Sheet 42 of 48

+APU_CORE



+APU_CORE_NB



capacitors under processor on bottom side of board